

# Computation Structures — Tutorial 10

November 24, 2015

## A Performance-Oriented $\beta$ Machine

1. Give the values of the various signals generated by the control logic when executing the following instructions: LD, ADD, BEQ.
2. Is it possible to add the following instructions to the instruction set of the  $\mu$ -code-less  $\beta$  machine? If yes, give the values of the various signals generated by the control logic when executing this instruction. Else, just explain why it cannot be implemented.

(a) PUSH(Rc, 4, Ra):

```
PC <- PC + 4
Mem[Reg[Ra]] <- Reg[Rc]
Reg[Ra] <- Reg[Ra] + 4
```

(b) LDA(Ra, Rb, Rc):

```
PC <- PC + 4
EA <- Reg[Ra] + Reg[Rb]
Reg[Rc] <- Mem[EA]
```

(c) STA(Ra, Rb, Rc):

```
PC <- PC + 4
EA <- Reg[Ra] + Reg[Rb]
Mem[EA] <- Reg[Rc]
```

(d) MVEQ(Ra, Rb, Rc):

```
PC <- PC + 4
if Reg[Ra] = 0 then Reg[Rc] <- Reg[Rb]
```

(e) MVCEQ(Ra, literal, Rc):

```
PC <- PC + 4
if Reg[Ra] = 0 then Reg[Rc] <- SEXT(literal)
```

(f) SWAP(Ra, literal, Rc):

```
PC <- PC + 4
EA <- Reg[Ra] + SEXT(literal)
TMP <- Mem[EA]
Mem[EA] <- Reg[Rc]
Reg[Rc] <- TMP
```

(g) TCLR(Ra, literal, Rc):

```
PC <- PC + 4
EA <- Reg[Ra] + SEXT(literal)
Reg[Rc] <- Mem[EA]
Mem[EA] <- 0
```

