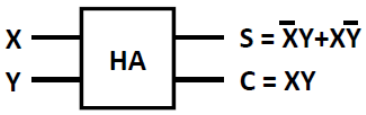
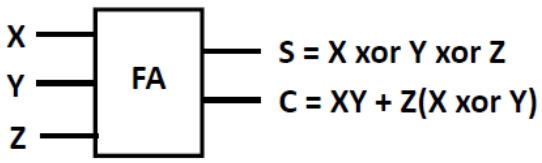
Composants logiques

Half adder = additionneur 2 bits

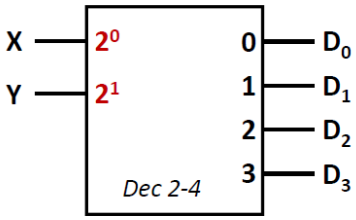


X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full adder = additionneur 3 bits



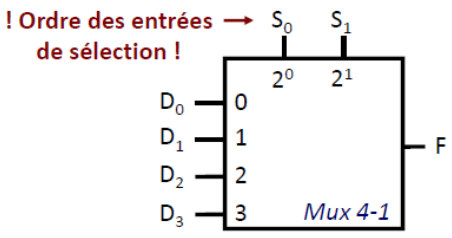
Décodeur = *générateur de minterms*



Y	X	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1
		$\bar{X}\bar{Y}$	$X\bar{Y}$	$\bar{X}Y$	XY

Multiplexeur = sélectionneur d'entrées

2^n entrées, **n** sélections → **1** sortie



S_1	S_0	F
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

$$F = \bar{S_1}\bar{S_0}D_0 + \bar{S_1}S_0D_1 + S_1\bar{S_0}D_2 + S_1S_0D_3$$

Portes universelles : NAND et NOR

- NAND : $F = \overline{A.B} = \bar{A} + \bar{B}$

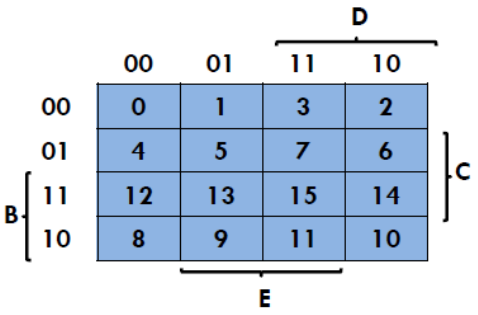
F = SOMME DE PRODUITS

- NOR : $F = \overline{A + B} = \bar{A}.\bar{B}$

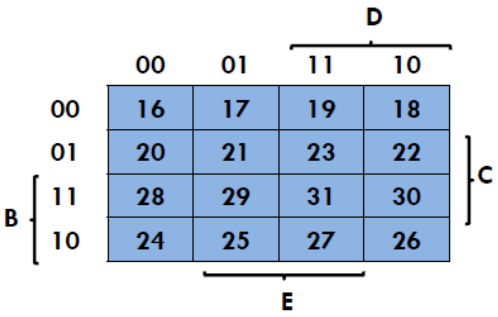
F = PRODUIT DE SOMMES

Karnaugh

5 variables



A = 0



A = 1