EXAM - June 2019

MICROELECTRONICS AND IC DESIGN (ELEN0037)

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1 Constants

$q = 1.602 \times 10^{-19}\, C$
$k = 1.38 \times 10^{-23}\, JK^{-1}$
$n_i = 1.1 \times 10^{16}\, carriers/m^3 \,@\, T = 300\, K$
n_i doubles for every 11°C increase in temperature
$n \times p = n_i^2$
$\varepsilon_0 = 8.854 \times 10^{-12} Fm^{-1}$
$K_{ox} \cong 3.9$
$K_s \cong 11.8$

2 Diode

$V_T = \frac{kT}{q} \cong 26\, mV \,@\, 300K$

2.1 Reverse-Biased

$Q = 2C_{j0}\Phi_0\sqrt{1 + \frac{V_R}{\Phi_0}}$
$C_j = \frac{C_{j0}}{\sqrt{1+\frac{V_R}{\Phi_0}}}$
$C_{j0} = \sqrt{\frac{qK_s\varepsilon_0}{2\Phi_0}\frac{N_A N_D}{N_A+N_D}}$
$C_{j0} = \sqrt{\frac{qK_s\varepsilon_0}{2\Phi_0}N_D}$ if $N_A \gg N_D$
$\Phi_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$

2.2 Forward-Biased

$I_D = I_S \exp\left(\frac{V_D}{V_T}\right)$
$I_S = A_D q n_i \left(\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D}\right)$

Small-Signal Model

$r_d = \frac{V_T}{I_D}$
$C_T = C_d + C_j$
$C_d = \tau_t \frac{I_D}{V_T}$
$C_j \cong 2C_{j0}$

3 N-channel MOSFET

For p-channel MOSFET, use the same equations as for the n-channel, with negative signs in front of all voltages.
$V_{eff} = V_{GS} - V_{tn}$
$V_{tn} = V_{tn-0} + \gamma\left(\sqrt{V_{SB} + 2\Phi_F} - \sqrt{2\Phi_F}\right)$
$\Phi_F = V_T \ln\left(\frac{N_A}{n_i}\right)$ (see diode equations for V_T)
$\gamma = \frac{\sqrt{2qK_s\varepsilon_0 N_A}}{C_{ox}}$
$C_{ox} = \frac{K_{ox}\varepsilon_0}{t_{ox}}$

3.1 Triode region ($V_{GS} > V_{tn}$, $V_{DS} \leq V_{eff}$)

$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^2}{2}\right]$

Small-Signal Model ($V_{DS} \ll V_{eff}$)

$r_{ds} = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{eff}-V_{DS})} \cong \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)V_{eff}}$
$C_{gd} = C_{gs} \cong \frac{1}{2}WLC_{ox} + WL_{ov}C_{ox}$
$C_{sb} = C_{db} = \frac{C_{j0}(A_s+WL/2)}{\sqrt{1+\frac{V_{sb}}{\Phi_0}}}$

3.2 Active (Pinch-Off) Region ($V_{GS} > V_{tn}$, $V_{DS} \geq V_{eff}$)

$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{tn})^2\left[1 + \lambda(V_{DS} - V_{eff})\right]$
$\lambda = \frac{k_{ds}}{2L\sqrt{V_{DS}-V_{eff}+\Phi_0}}$
$k_{ds} = \sqrt{\frac{2K_s\varepsilon_0}{qN_A}}$
$V_{eff} = V_{GS} - V_{tn} = \sqrt{\frac{2I_D}{\mu_n C_{ox} W/L}}$

Small-Signal Model

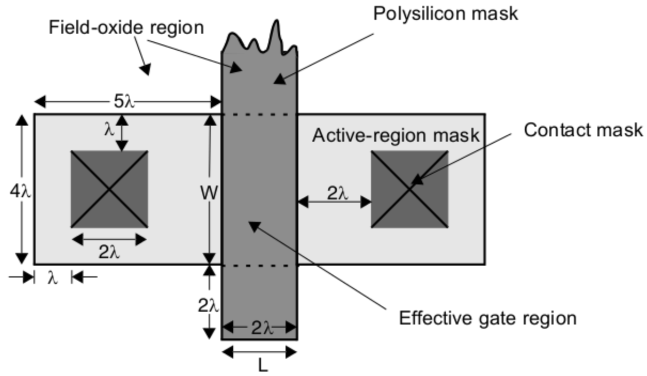
$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox}\left(\frac{W}{L}\right)V_{eff} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)I_D} = \frac{2I_D}{V_{eff}}$
$g_s = \frac{\partial I_D}{\partial V_{SB}} = \frac{\gamma g_m}{2\sqrt{V_{SB}+2\Phi_F}}$
$r_{ds} = \frac{\partial V_{DS}}{\partial I_D} \cong \frac{1}{\lambda I_D}$
$C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox} = \frac{2}{3}WLC_{ox} + WC_{gs-ov}$
$C_{gd} = WL_{ov}C_{ox} = WC_{gd-ov}$
$C_{sb} = (A_s + WL)C_{js} + P_s C_{j-sw}$
$C_{js} = \frac{C_{j0}}{\sqrt{1+\frac{V_{sb}}{\Phi_0}}}$
$C_{db} = A_d C_{jd} + P_d C_{j-sw}$
$C_{jd} = \frac{C_{j0}}{\sqrt{1+\frac{V_{db}}{\Phi_0}}}$

3.3 Default values for MOSFET ($0.8\,\mu m$)

n-channel	$T = 300K$ (Room temperature)	p-channel
$\mu_n C_{ox} = 92\mu A/V^2$		(30)
$V_{tn-0} = 0.8V$		($V_{tp-0} = -0.9V$)
$\gamma = 0.5V^{1/2}$		(0.8)
$r_{ds}(\Omega) = 8000L(\mu m)/I_D(mA)$ in active region		(12000)
$C_{js} = C_{jd}(= C_j) = 2.4 \times 10^{-4}pF/(\mu m)^2$		(4.5×10^{-4})
$C_{j-sw} = 2.0 \times 10^{-4}pF/\mu m$		(2.5×10^{-4})
$C_{ox} = 1.9 \times 10^{-3}pF/(\mu m)^2$		(1.9×10^{-3})
$C_{gs-ov} = C_{gd-ov} = 2.0 \times 10^{-4}pF/\mu m$		(2.0×10^{-4})

4 Design rules

The design rules are expressed in terms of a quantity, λ, where λ is $1/2$ the minimum permitted gate length ($L = 2\lambda$). The corresponding layout of the active, polysilicon, and contact masks of the smallest transistor that can be realized in a given process when a contact must be made to each junction is summarized hereafter



The n well surrounds the p-channel MOST, by at least 3λ. The minimum spacing between the n well and the junctions of n-channel MOST is 5λ. Therefore, the closest an n-channel MOST can be placed to a p-channel MOST is 8λ. The minimum widths of poly, metal 1, and metal 2 are 2λ, 2λ, and $\lambda 3$, respectively.

5 Filters

5.1 First order

General form $\quad H(s) = \dfrac{k_1 s + k_0}{s + \Omega_0}$

Low Pass $\quad H(s) = \dfrac{\Omega_0}{s + \Omega_0}$

High Pass $\quad H(s) = \dfrac{s}{s + \Omega_0}$

5.2 Second order (Biquad)

General form $\quad H(s) = \dfrac{k_2 s^2 + k_1 s + k_0}{s^2 + (\Omega_0/Q)\, s + \Omega_0^2}$

Low Pass $\quad H(s) = \dfrac{\Omega_0^2}{s^2 + (\Omega_0/Q)\, s + \Omega_0^2}$

Band Pass $\quad H(s) = \dfrac{(\Omega_0/Q)\, s}{s^2 + (\Omega_0/Q)\, s + \Omega_0^2}$

Band Stop $\quad H(s) = \dfrac{s^2 + \Omega_0^2}{s^2 + (\Omega_0/Q)\, s + \Omega_0^2}$

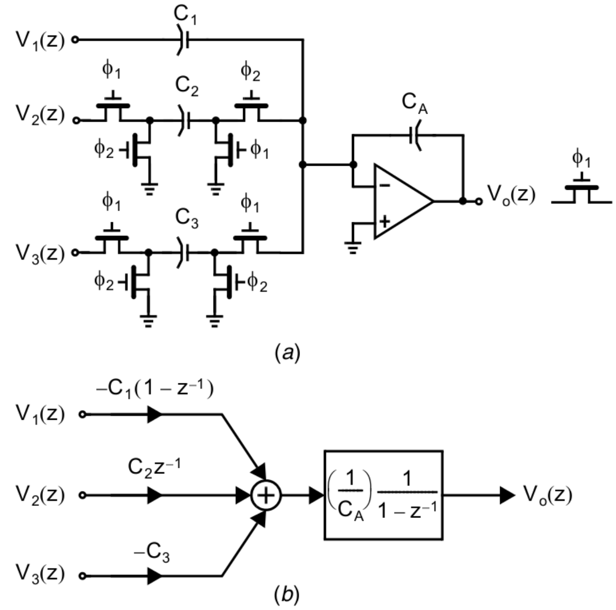
High Pass $\quad H(s) = \dfrac{s^2}{s^2 + (\Omega_0/Q)\, s + \Omega_0^2}$

6 Z transform

Exact transform	Bilinear transform
$z = e^{j\omega T}$	$s = \frac{z-1}{z+1}$, $z = \frac{1+s}{1-s}$
$z \simeq 1 + j\omega T$ if $\omega T \ll 1$	$\Omega_{s-domain} = \tan\left(\frac{\omega_{z-domain}}{2}\right)$

7 Switched-capacitor ciruits

7.1 Signal-Flow-Graph Analysis



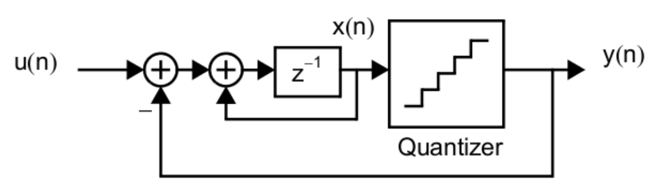
8 Data converters

Number of bits: N, number of levels: $L = 2^N$, quantization error: $\Delta = \frac{V_{ref}}{L}$, RMS error: $e_{rms} = \Delta/\sqrt{12}$, oversampling rate: $OSR = \frac{f_s}{2f_0}$.

Converter type	Signal to noise ratio $SQNR_{max}$
Nyquist rate ($OSR = 1$)	$6.02N + 1.76$
Oversamp., no noise shaping	$6.02N + 1.76 + 10 \log OSR$
Oversamp., 1^{st}-order noise shaping	$6.02N + 1.76 - 5.17 + 30 \log OSR$
Oversamp., 2^{nd}-order noise shaping	$6.02N + 1.76 - 12.9 + 50 \log OSR$

These formulae are valid (1) for an input sine wave (otherwise remove the +1.76 term), and (2) when the input signal spans the full range of the converter.

8.1 first-order ΣΔ modulator



The state equations of the first-order ΣΔ modulator are given by:

$$\begin{aligned} y(n) &= Q(x(n)) \\ e(n) &= y(n) - x(n) \\ x(n+1) &= x(n) + u(n) - y(n) \end{aligned}$$

9 Noise Analysis and Modeling

Spectral Density: $V_n^2(f) \quad [V^2/Hz]$.
Root Spectral Density: $V_n(f) \quad [V/\sqrt{Hz}]$.
Total noise power: $V_n^2 = \int_0^\infty V_n^2(f)\, df \quad [V^2]$.

Sum of two noise sources

$$V_n^2 = V_{n1}^2 + V_{n2}^2 + 2CV_{n1}V_{n2},$$

$$P_n = P_{n1} + P_{n2} + 2C\sqrt{(P_1 P_2)}.$$

White noise: $V_n^2(f) = k_w^2$
Pink (Flicker or $\frac{1}{f}$) noise: $V_n^2(f) = \frac{k_f^2}{f}$
Filtered noise: $V_{no}^2(f) = |A(f)|^2 V_{ni}^2(f)$
Voltage noise across a resistor: $V_R^2(f) = 4kTR$
Accumulated Voltage noise across a capacitor: $V_C^2 = \frac{kT}{C}$
Accumulated Current noise across an inductor: $I_L^2 = \frac{kT}{L}$

10 Miscellaneous

Matching accuracy for capacitors

We desire to match C_1 and C_2, such that $K = \frac{C_2}{C_1} \geq 1$.
Analysis gives the condition $\frac{P_1}{A_1} = \frac{P_2}{A_2}$.
Therefore $K = \frac{C_2}{C_1} = \frac{A_2}{A_1} = \frac{P_2}{P_1}$.
If C_1 is a square of size $x_1 \times x_1$, and C_2 has size $x_2 \times y_2$, we have:

$$y_2 = x_1\left(K \pm \sqrt{(K^2 - K)}\right)$$

$$x_2 = K\frac{x_1^2}{y_2}$$

Square resistance

$R_\square = \frac{\rho}{H} = \frac{1}{q\mu_n N_D H}$
$R = R_\square \frac{L}{W}$

Signal to noise ratio (SNR), decibels

$SNR = 10\log\left(\frac{P_{signal}}{P_{noise}}\right) \qquad [dB]$
Conversion from power to dB: $10\log(P)$
Conversion from power to dBm (dB mW): $10\log\left(\frac{P}{1mW}\right)$
Conversion from voltage to dB: $20\log(V)$
Conversion from voltage to dBm (dB mV): $20\log\left(\frac{V}{1mV}\right)$

Steady state percentage value of first order filter versus time constant τ

Time	Percentage
τ	63%
2τ	86%
3τ	95%
4τ	98%
5τ	99%