Electromagnetic Compatibility Tips for Power Converters

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A power supply design story from Robert A. Pease

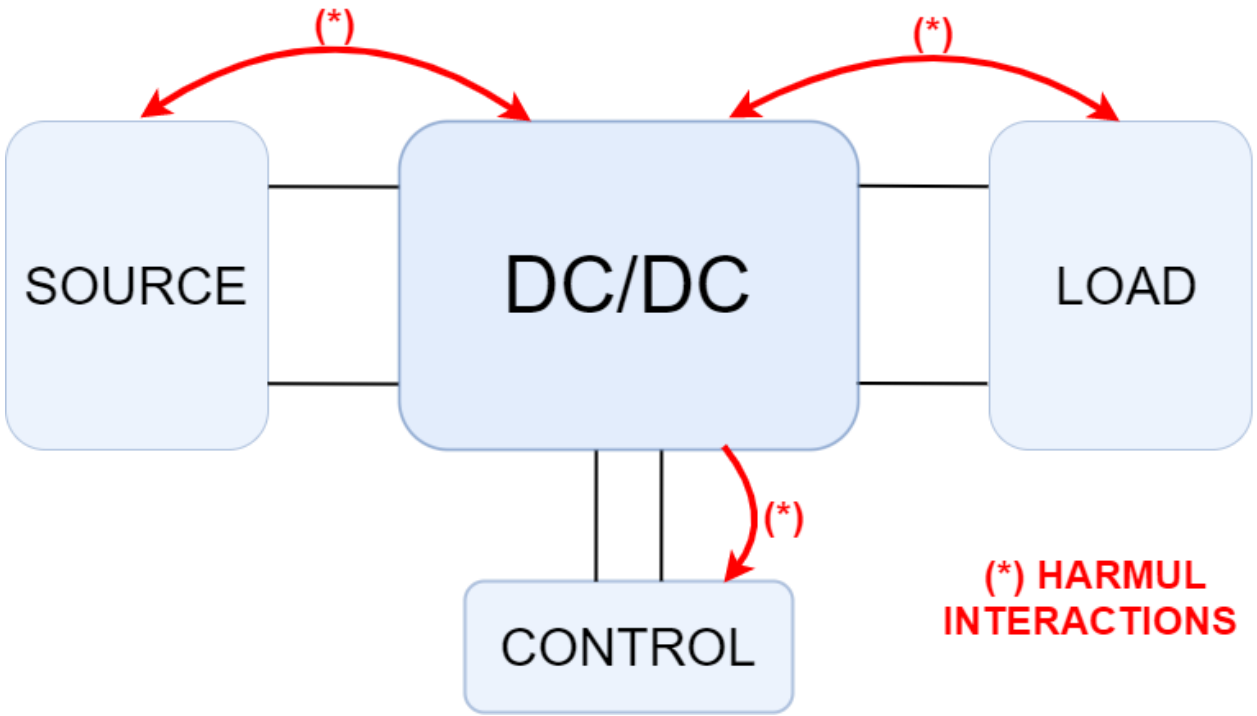
One of the stories that keeps rattling around the industry is about a group of engineers who decide to band together and start a new computer company. The smartest one is assigned to do the main processor board. Another smart engineer does all the interfaces. And the smart but green "kid engineer" is assigned to do the switch-mode power supply because, of course, that's the easiest part to do. (Anybody who has worked on a big switcher will probably speak up right away: The switcher is *not* as easy as it seems.) In the end, the power-supply design takes a lot longer than everybody expects.

One day, the young engineer opens up the compartment where the balky power supply resides, and it blows up in his face. After his co-workers take the poor fellow to the hospital, they ask around and find a consulting engineer who makes a living out of fixing exactly this kind of switcher problem. The switcher design was slightly off-course and needed the hand of an expert before it would work correctly. So remember, designing switchers is no simple task. Don't hesitate to call in an expert. Note, if this story were not substantially true, the consulting engineer would have starved to death, long ago. I rest my case.

Why worrying? (Robert A. Pease)

drawing board—even if we're really good at designing other circuits. After all, a switcher is a complicated system composed of power transistors, transformers, inductors, one or more control ICs, and lots of other passive components. And, the circuit's layout is critical: The layout must guard small signals against electrostatic interference and cross-talk, and, even more importantly, must control and reject the electromagnetic strays. I mean, for a switcher to be efficient, the volts per microsecond and amperes per microsecond get really *large*, so it doesn't take many picofarads or nanohenries to couple a big noise into the rest of the circuit. The paths for high currents are important, and the paths for cooling air are even more critical.

Introduction: what is the "EMC problem"?



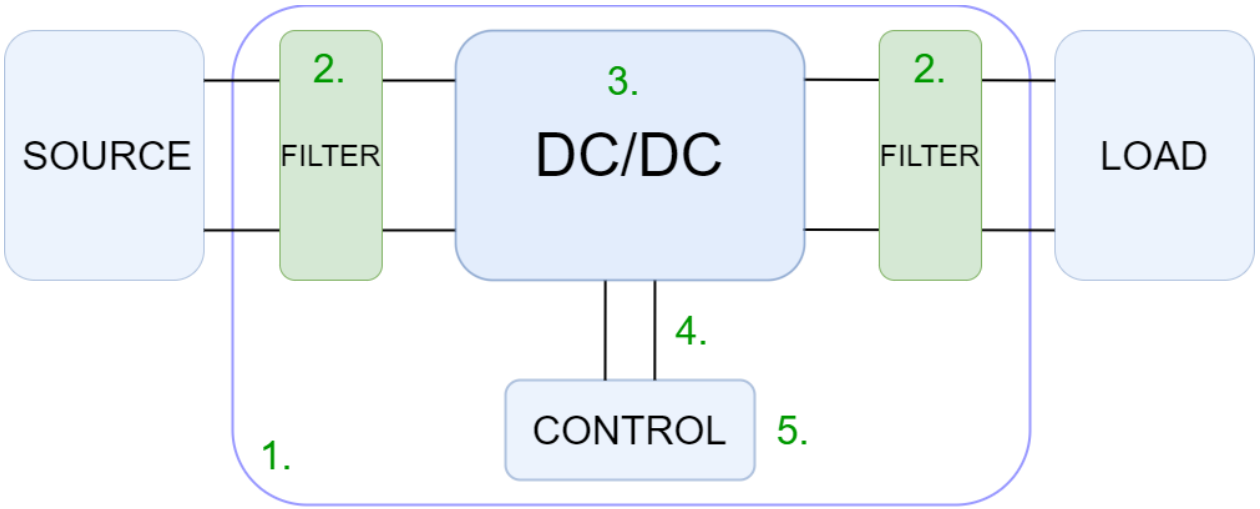
- Harmful and unexpected interactions are present.
- A lot of consequences are possible:
  1. perturbation of the power source/load,
  2. malfunction of the DC/DC controller,
  3. failure...

Introduction: some concepts

- Emission (agressor side): the "device" generates electromagnetic interferences to the outside world.
- Immunity (victim side): the "device" is perturbed by the outside world and should resist to the perturbations.
- Types of unwanted interactions:
  1. conducted interferences (U/I),
  2. radiated interferences (EM waves) and,
  3. near field coupling (E/H).

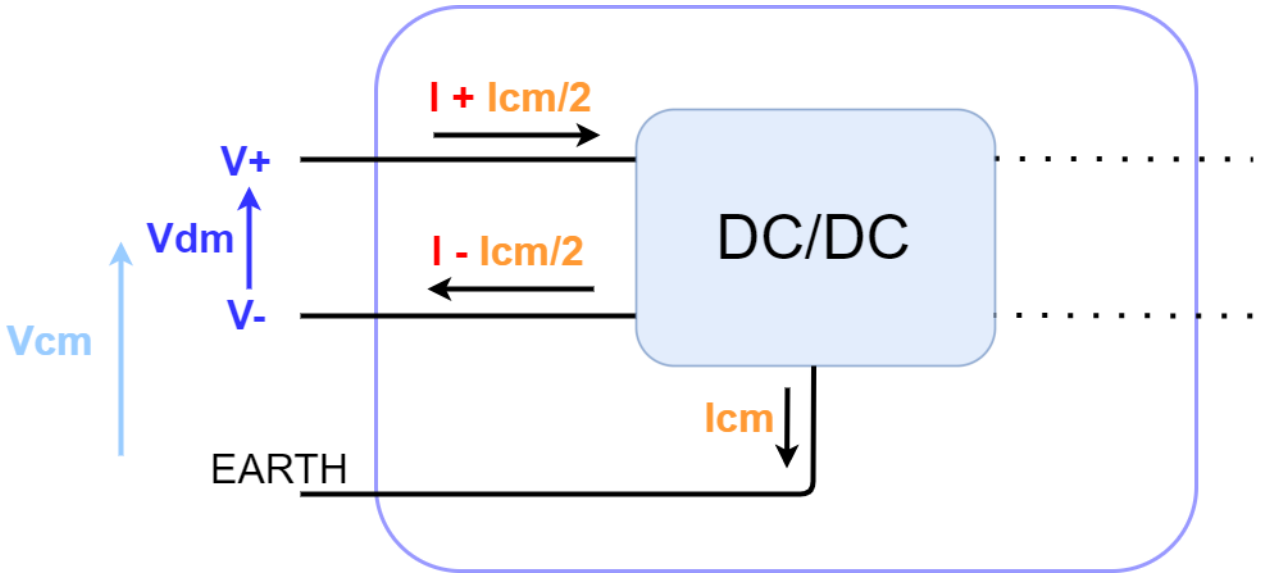
Each discussed topic could take hours but the goal of the course is to provide a minimum toolkit.
Anyway, always use scientific approach to EMC problems, use your brain modeler and simulator and perform measurements to access your understanding.
Interference finally act on your circuit as equivalent voltage or current sources to be identified.

Introduction: the typical solutions



1. A metallic shield prevents radiated interferences.
2. Input and output filters prevent conducted/radiated interferences.
3. Near field emission has to be minimized in the power part.
4. Unwanted signal coupling between power and control parts has to be minimized by proper layout.
5. Control design has to be robust against interferences.

Conducted interferences: common vs. differential mode



- Common mode voltage: $Vcm = (V_+ + V_-)/2$
- Differential mode voltage: $Vdm = (V_+ - V_-)$
- Common mode current: Icm
- Differential mode current: $Idm = I$

Conducted interferences: filter example

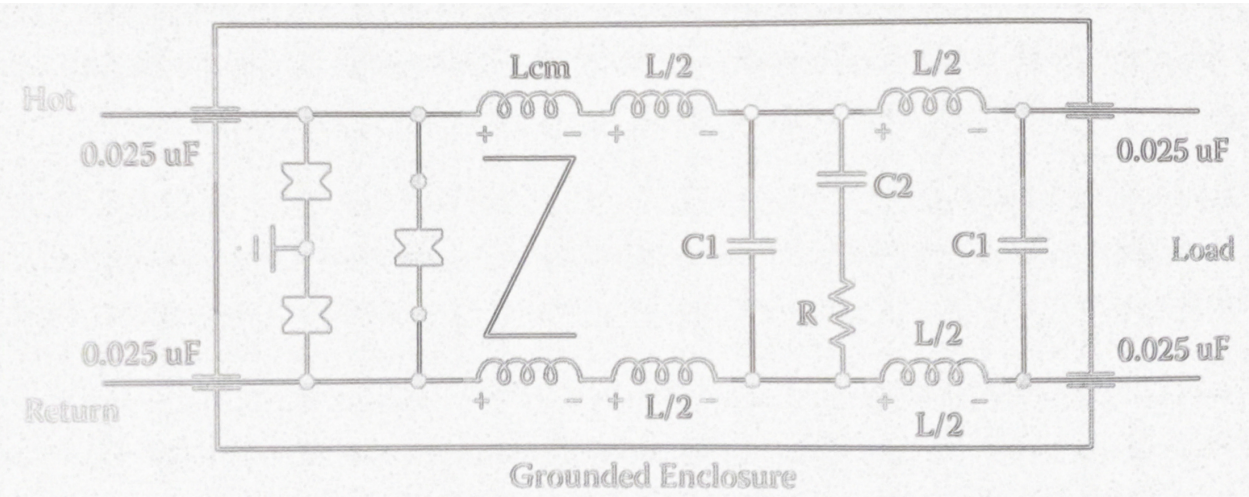


Figure: Excerpt of [1]

The filter includes:

- a common mode part (inductor + capacitor),
- a differential mode part (inductor + capacitor) and,
- some damping.

Conducted interferences are reduced on the incoming and outgoing wires, therefore radiated emission is also reduced.

Conducted interferences: filter and negative resistance

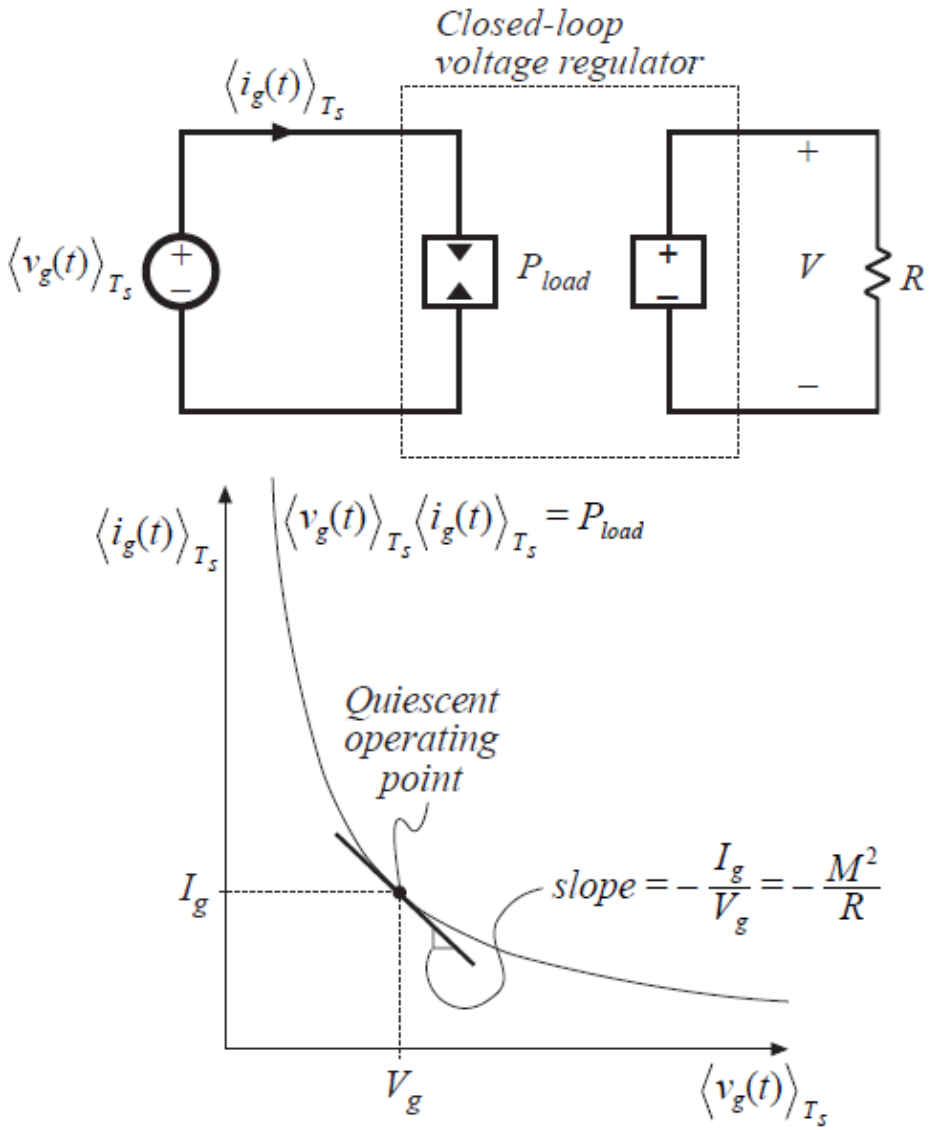


Figure: Excerpt of [2]

Conducted interferences: filter design rules

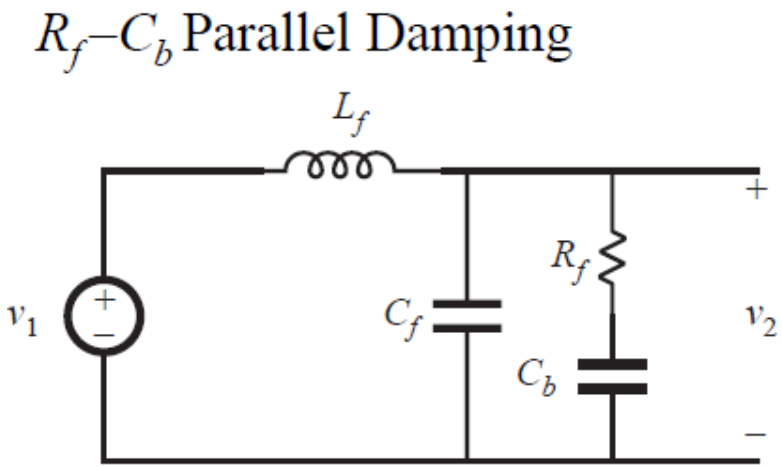


Figure: Excerpt of [2].

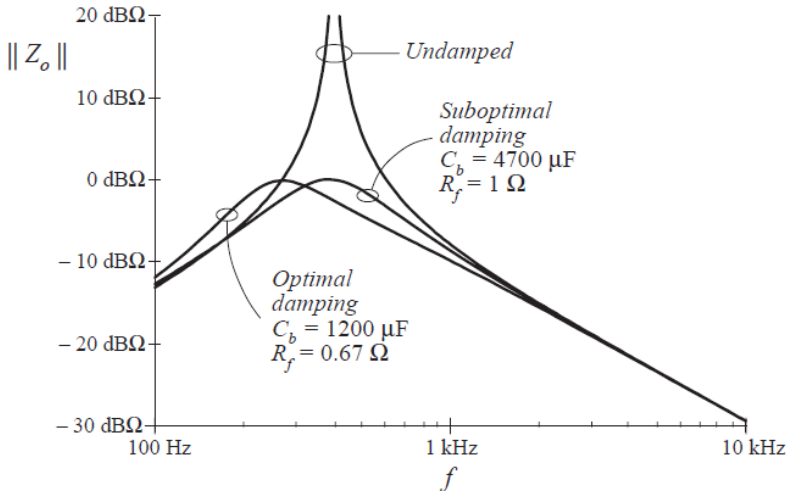


Figure: Excerpt of [2].

- Pole placement gives the required attenuation.
- Use a characteristic impedance far lower than the converter negative resistance.
- Correctly damp the filter (see [2] chapter 10, paragraph 10.4.1).

Interference sources: the switching cell

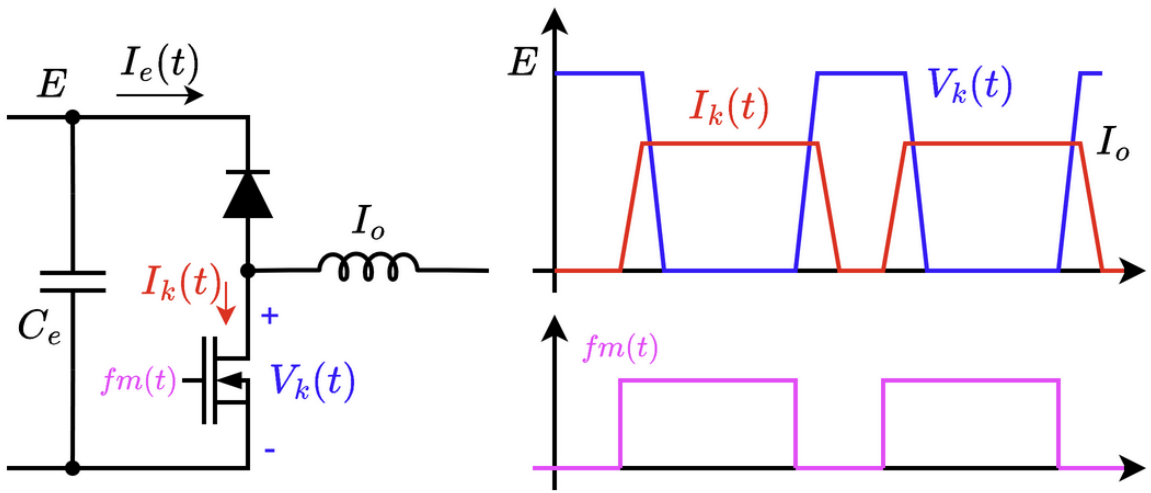


Figure: Excerpt of [3]

- E and I_o are constant external parameters (small ripple approximation)
- Two interference sources have to be considered:
  - $V_k(t) = fm(t) \cdot E$
  - $I_e(t) = fm(t) \cdot I_o$

Interference sources: the switching cell

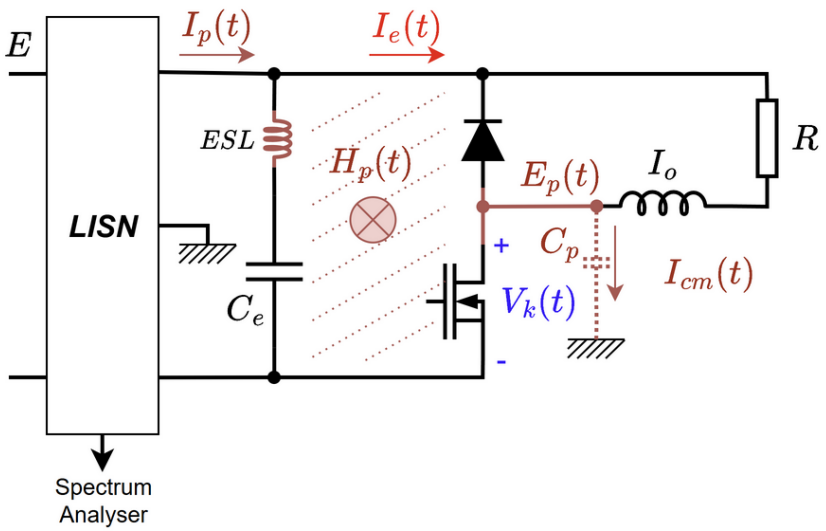
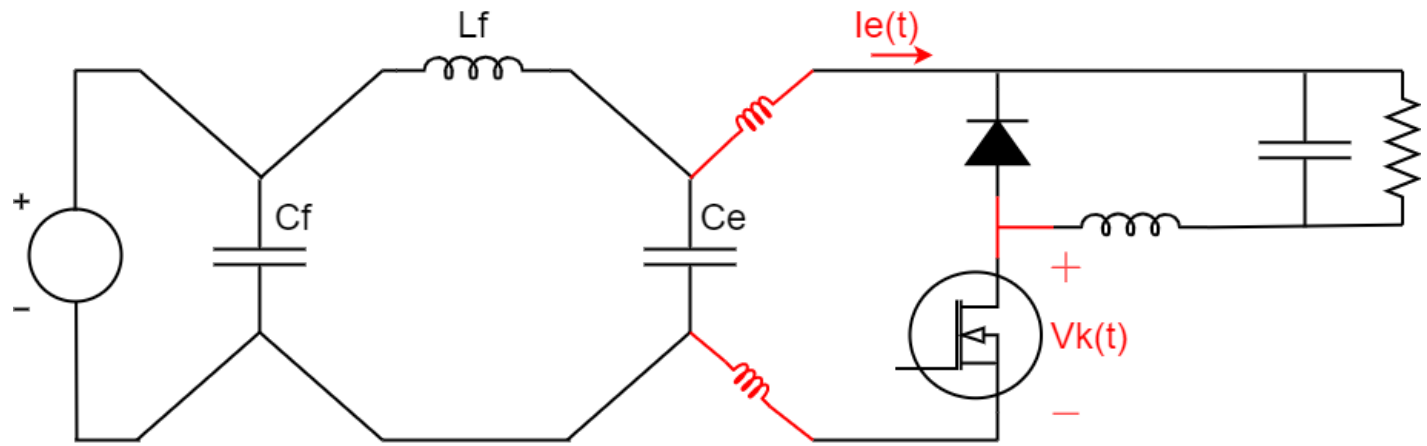


Figure: Excerpt of [3]

- $\frac{dV_k(t)}{dt} \Rightarrow \frac{dE_p(t)}{dt} \Rightarrow$
  - capacitive coupling $\Rightarrow I_{cm}(t)$
  - high impedance EM wave generation
- $\frac{dI_e(t)}{dt} \Rightarrow$ voltage across ESL of C_e appears $\Rightarrow$ conducted emission
- $\frac{dI_e(t)}{dt} \Rightarrow \frac{dH_p(t)}{dt} \Rightarrow$
  - magnetic near field coupling
  - low impedance EM wave generation

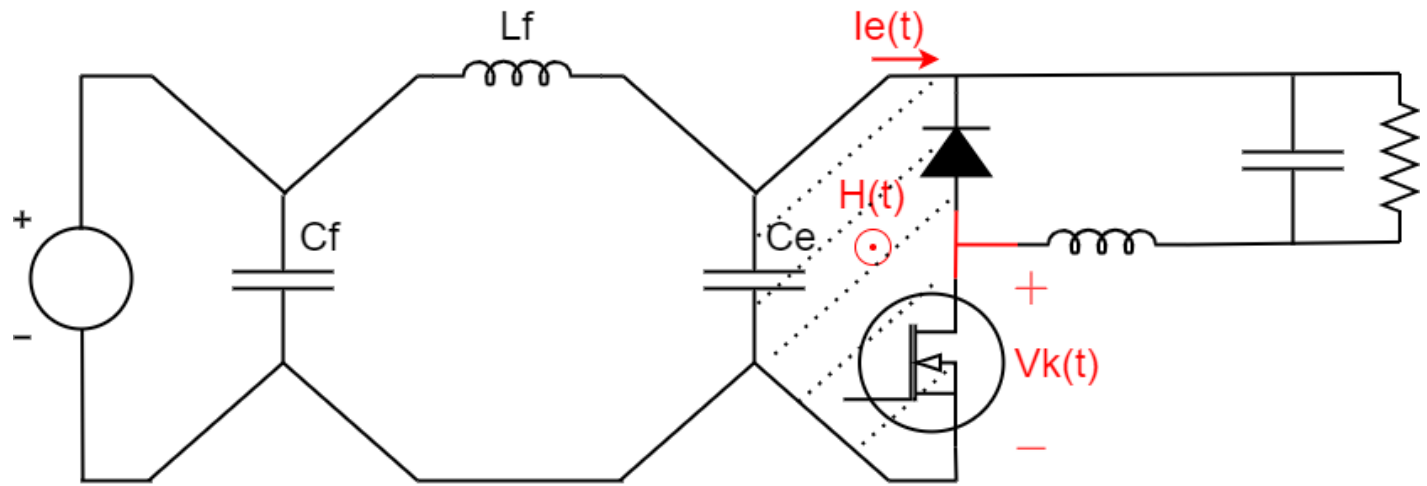
- $V_k(t)$ is subject to high $\frac{dV_k}{dt}(1 - 50kV/\mu s)$
- $I_e(t)$ is subject to high $\frac{dI_e}{dt}(100 - 1000A/\mu s)$

Interference coupling: equivalent Series Inductance (ESL) mitigation



- Add a differential mode filter (Lf, Cf).
- Connect capacitors using VEEING to reduce ESL effect associated voltage.
- Use low ESR capacitors (film, ceramic).
- The problem is far less critical on the output of the buck converter because...

Interference coupling: reduction of generated magnetic field



$Ie(t)$ has high $\frac{dIe(t)}{dt} \Rightarrow H(t)$ has high $\frac{dH(t)}{dt}$. Therefore, a large $A\mu_0 \frac{dH(t)}{dt} = \frac{d\Phi(t)}{dt}$ exists and creates emf in surrounding circuit loops of area A.

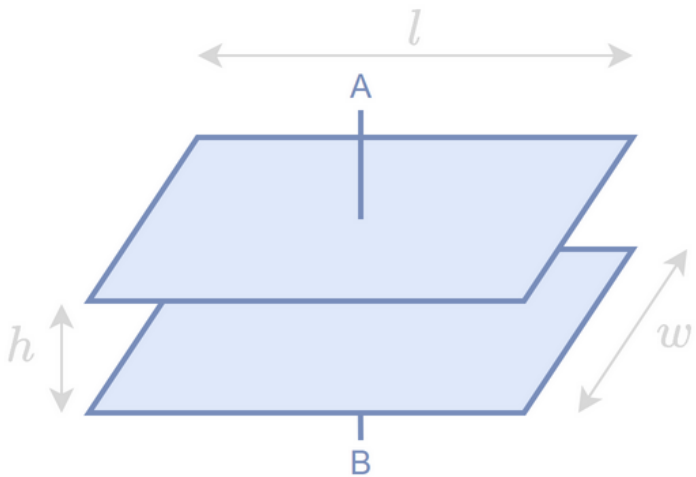
Rule: minimize the surface of loops with high $\frac{dIe(t)}{dt}$

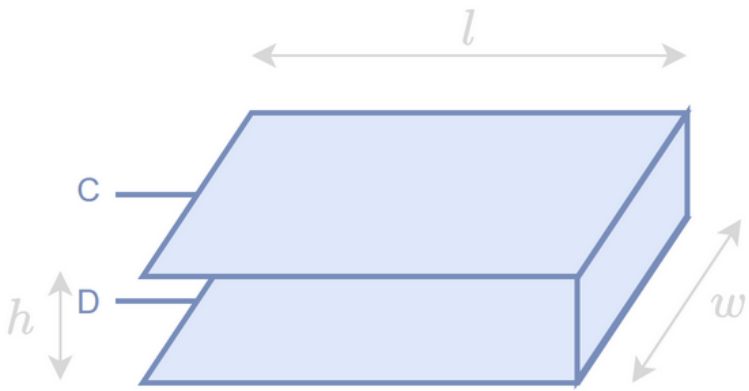
- minimize loops with clever layout,
- add an extra wire to improve an existing circuit or,
- use a ground plane.

Note about leakage inductances calculation

Possible solutions are:

- reduce the loop of high $\frac{dIe(t)}{dt}$,
- as a rule of thumb estimate L_{leak} between 5 and $10nH/cm$,
- refine your model using EM tools or formulae.

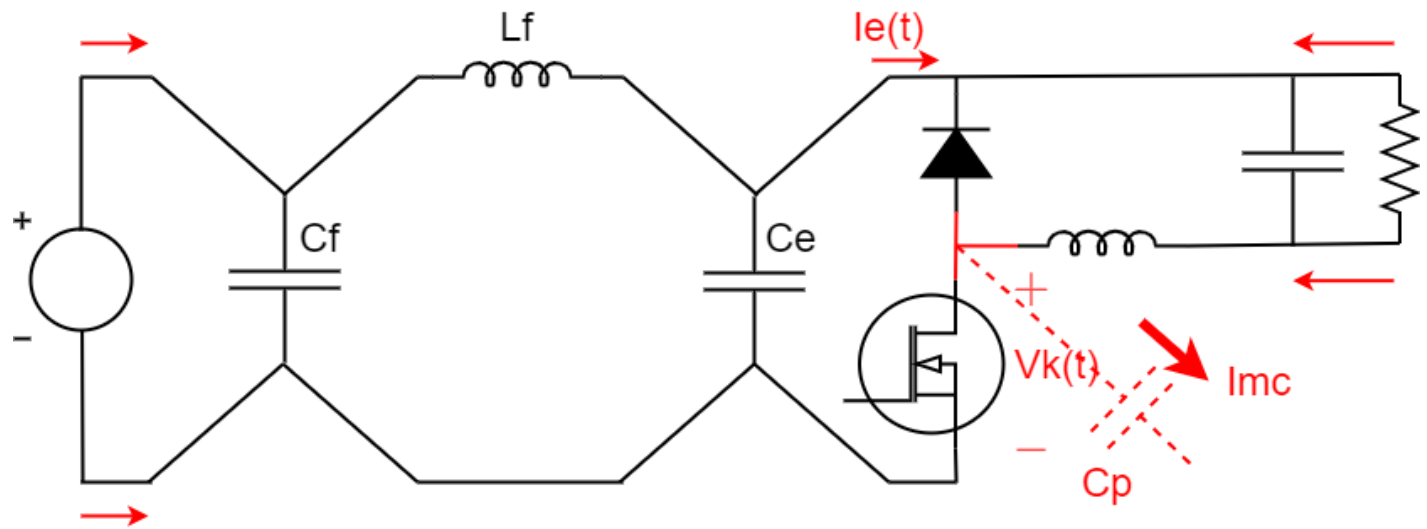




$$C_{A-B} = \epsilon_r \epsilon_0 \frac{l\,w}{h}$$

$$L_{C-D} = \mu_r \mu_0 \frac{l\,h}{w}$$

Interference coupling: capacitive coupling

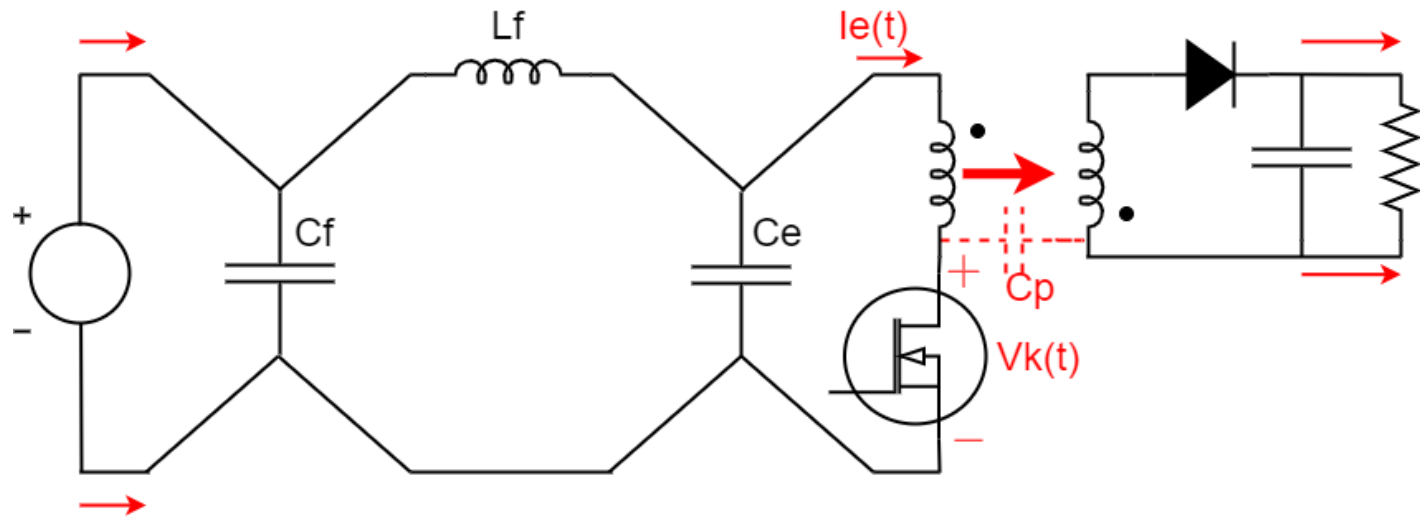


Example: Vk(t) switches in 25 ns from 0 to 24 V.
$I_{Cp} = Cp\frac{dV(t)}{dt} = 1pF\frac{24V}{25ns} = 1mA$ for Cp as low as $1pF$.

Rule: reduce the surface of copper tracks with high $\frac{dVk(t)}{dt}$

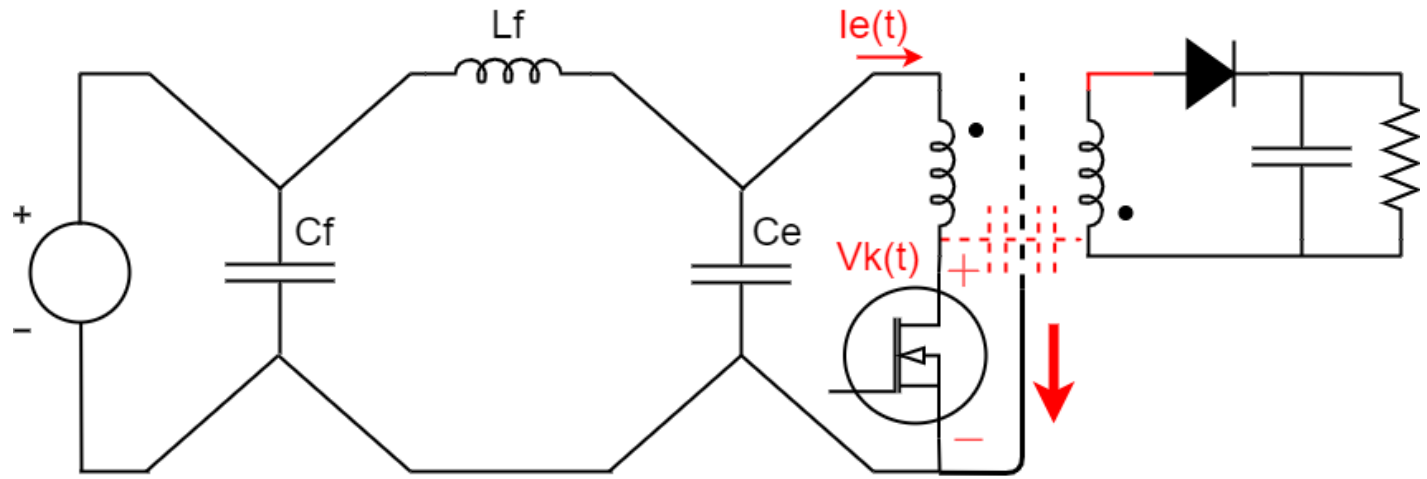
- reduce the surface of copper tracks with high $\frac{dVk(t)}{dt}$ and put sensitive circuits apart from them,
- use the last layer of an inductor winding as a shield,
- add electrical insulation on the heatsink.

Interference coupling: capacitive coupling in transformers



Remember that high $\frac{dVk(t)}{dt}$ node also couple through the transformer windings.

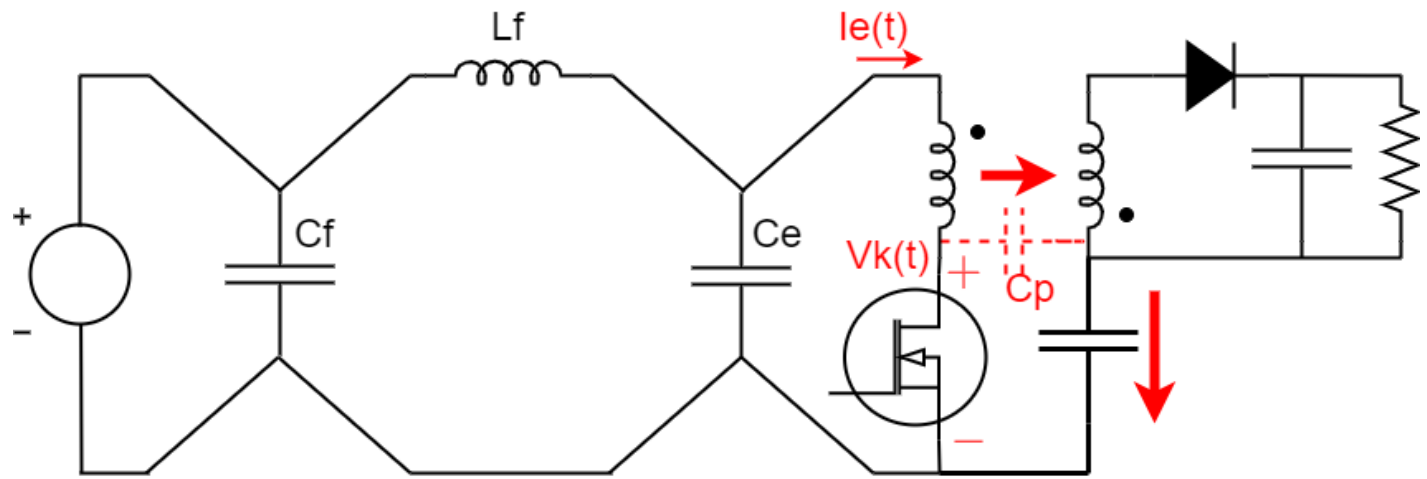
Capacitive coupling in transformers solution 1



Rule: provide a return current path

- The shield provides a return current path for current generated by high $\frac{dVk(t)}{dt}$ that circulates through transformer parasitic capacitances.
- If the secondary winding of the transformer also creates a high voltage variation, a second shield is required.
- The shield is typically connected to the highest voltage winding because it creates the higher $\frac{dVk(t)}{dt}$.

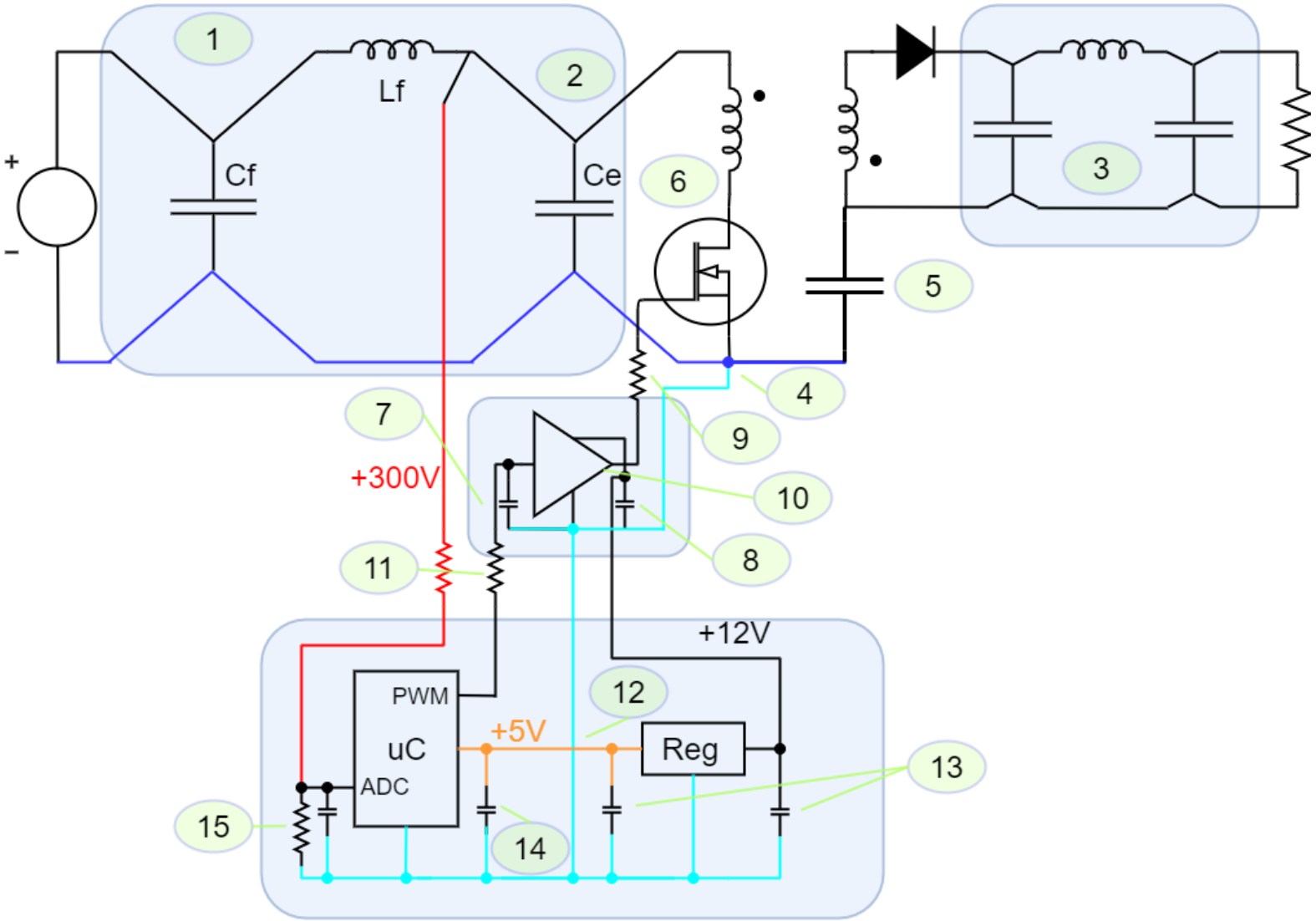
Capacitive coupling in transformers solution 2



Rule: provide a return current path

- The added capacitor provides a return current path for current generated by high $\frac{dVk(t)}{dt}$ that circulates through transformer parasitic capacitances.

Summary of construction rules



Summary of construction rules I

1. add an input filter,
2. use VEEING,
3. add an output filter,
4. separate power and control ground and connect them in one point, clearly separate power part and control part of the converter,
5. use a shield or a capacitor to provide a return path for capacitive currents,
6. minimize high $dIe(t)/dt$ loop area,
7. add a filtering capacitor at the input of the transistor driver (100 pF),
8. use a decoupling capacitor for the transistor driver,
9. add a small series resistor to drive the transistor,
10. place the transistor driver quite close to the transistor,

Summary of construction rules II

11. add a series resistor at the input of the driver,
12. creates the power supply of the uC locally on control side,
13. add decoupling capacitors for the voltage regulator,
14. add decoupling capacitors for the uC,
15. filter analog inputs of the uC.

References I

[1] R. L. Ozenbaugh, *EMI Filter Design*.
CRC Press, third ed., 2012.

[2] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*.
Kluwer Academic Publishers, second ed., 2001.

[3] F. Costa, C. Gautier, E. Labour, and B. Revol, *Electromagnetic Compatibility in Power Electronics*.
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References II

See also:

- ELEN0448-1, Applied Electricity and Electronics, Redouté Jean-Michel, Vanderbemden Philippe
- Certificat Interuniversitaire en Électronique de l'Énergie, https://web.umons.ac.be/fpms/fr/formations/cu-eleneg-c/