Elements of Power Electronics
PART I: Bases

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Goal and expectations

The goal of the course is to provide a toolbox that allows you to:

- understand power electronics concepts and topologies,
- to model a switching converter,
- to build it (including its magnetic components) and,
- to control it (with digital control).

Power Electronics is a huge area and the correct approach is to focus on **understanding** concepts.

Organization and material

The course is divided in three parts:

- PART I: Bases
- PART II: Digital control
- PART III: Topologies and applications

In PART I and PART III, chapters are numbered according to the reference book [1].
In PART II, chapters are numbered according to the reference book [2].

PART I: Bases

Chapter 1: Introduction

Fundamentals of Power Electronics

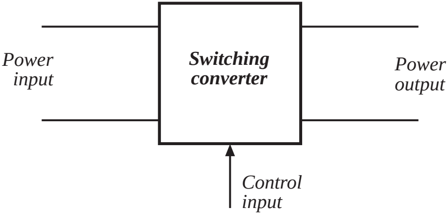
Second edition

Robert W. Erickson

Dragan Maksimovic

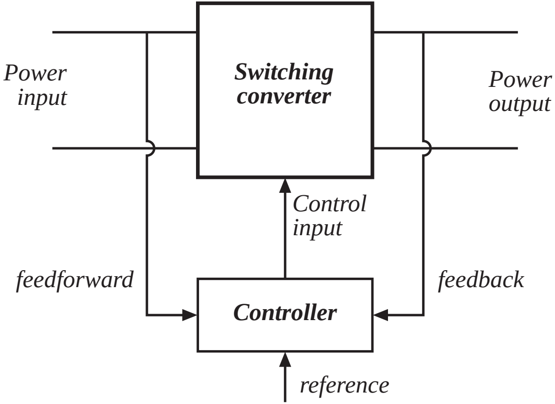
University of Colorado, Boulder

1.1 Introduction to Power Processing



Dc-dc conversion:	Change and control voltage magnitude
Ac-dc rectification:	Possibly control dc voltage, ac current
Dc-ac inversion:	Produce sinusoid of controllable magnitude and frequency
Ac-ac cycloconversion:	Change and control voltage magnitude and frequency

Control is invariably required



High efficiency is essential

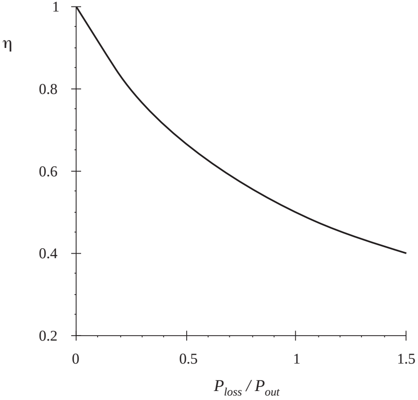
$$\eta = \frac{P_{out}}{P_{in}}$$

$$P_{loss} = P_{in} - P_{out} = P_{out}\left(\frac{1}{\eta} - 1\right)$$

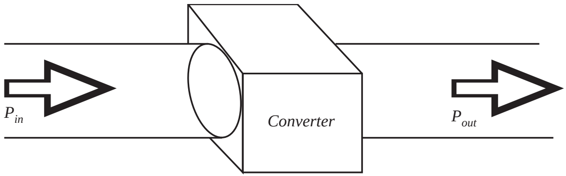
High efficiency leads to low power loss within converter

Small size and reliable operation is then feasible

Efficiency is a good measure of converter performance

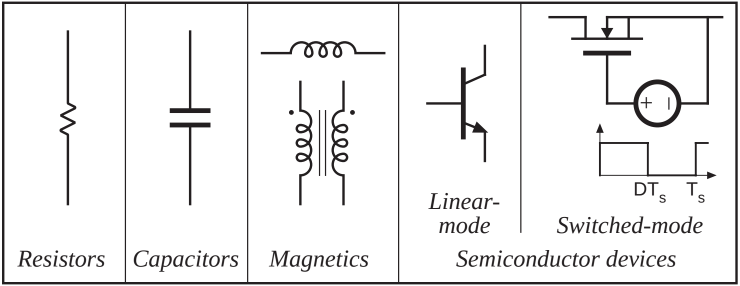


A high-efficiency converter

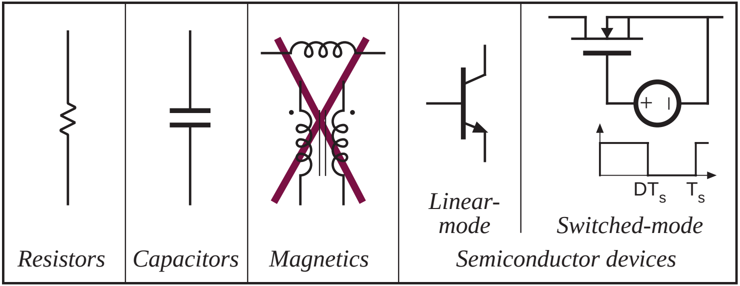


A goal of current converter technology is to construct converters of small size and weight, which process substantial power at high efficiency

Devices available to the circuit designer

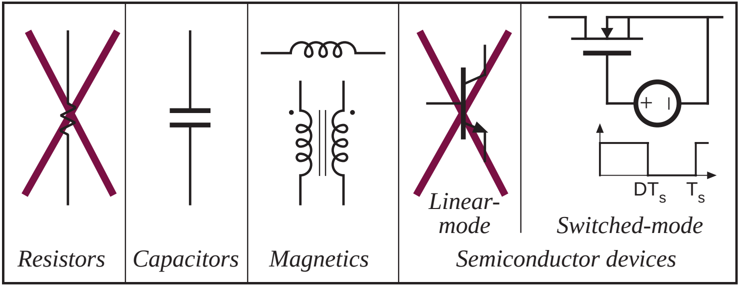


Devices available to the circuit designer



Signal processing: avoid magnetics

Devices available to the circuit designer



Power processing: avoid lossy elements

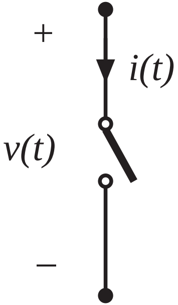
Power loss in an ideal switch

Switch closed: $v(t) = 0$

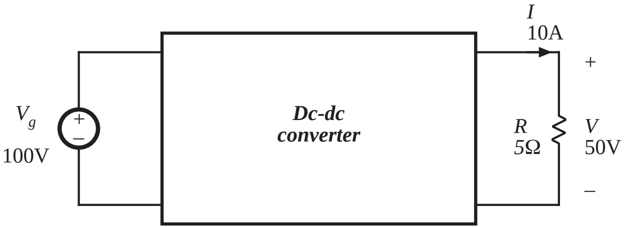
Switch open: $i(t) = 0$

In either event: $p(t) = v(t)\ i(t) = 0$

Ideal switch consumes zero power



A simple dc-dc converter example



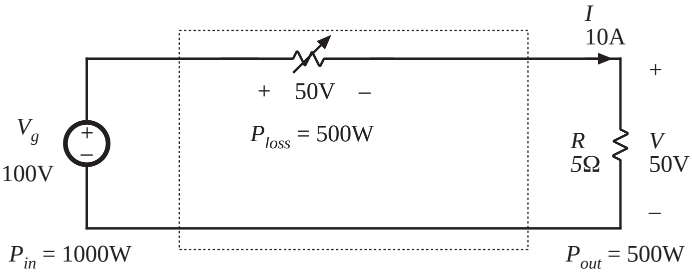
Input source: 100V

Output load: 50V, 10A, 500W

How can this converter be realized?

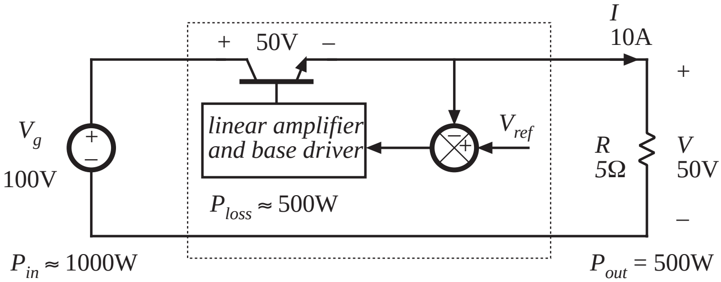
Dissipative realization

Resistive voltage divider



Dissipative realization

Series pass regulator: transistor operates in active region



Solutions?

- Can we find a better (more efficient) solution than the resistive voltage divider?
- What can we do to increase the voltage ($V > V_g$)?
- How can we create a galvanic isolation between the source and the load?

We will answer these questions in the following chapters.

1.2 Several applications of power electronics

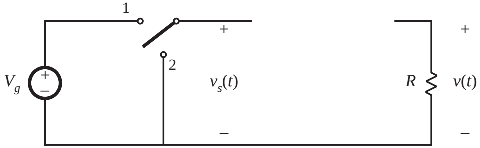
Power levels encountered in high-efficiency converters

- less than 1 W in battery-operated portable equipment
- tens, hundreds, or thousands of watts in power supplies for computers or office equipment
- kW to MW in variable-speed motor drives
- 1000 MW in rectifiers and inverters for utility dc transmission lines

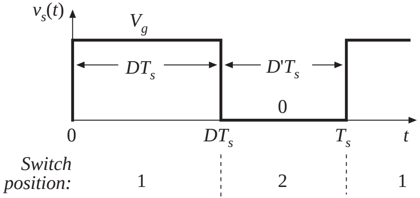
- 2.1 Introduction
- 2.2 Inductor volt-second balance, capacitor charge balance, and the small ripple approximation
- 2.3 Boost converter example
- 2.4 Cuk converter example
- 2.5 Estimating the ripple in converters containing twopole low-pass filters
- Addendum: Inductor volt-second balance, capacitor charge balance, the fast way
- 2.6 Summary of key points

2.1 Introduction
Buck converter

SPDT switch changes dc component



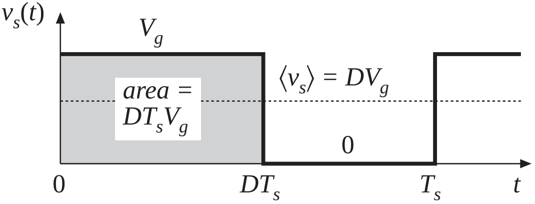
Switch output voltage waveform



Duty cycle *D:*
$0 \le D \le 1$

complement D′:
$D' = 1 - D$

Dc component of switch output voltage



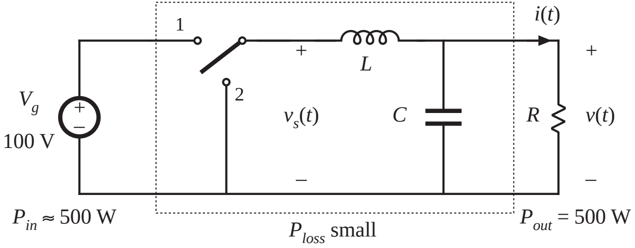
Fourier analysis: Dc component = average value

$$\langle v_s \rangle = \frac{1}{T_s}\int_0^{T_s} v_s(t)\, dt$$

$$\langle v_s \rangle = \frac{1}{T_s}\,(DT_sV_g) = DV_g$$

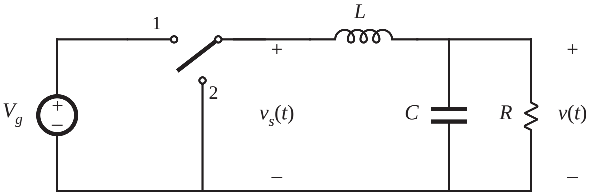
Addition of low pass filter

Addition of (ideally lossless) L-C low-pass filter, for removal of switching harmonics:

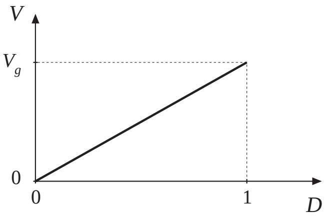


- Choose filter cutoff frequency f_0 much smaller than switching frequency f_s
- This circuit is known as the "buck converter"

Insertion of low-pass filter to remove switching harmonics and pass only dc component

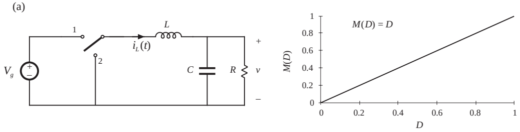


$$v \approx \langle v_s \rangle = DV_g$$

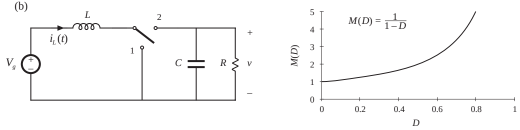


Three basic dc-dc converters

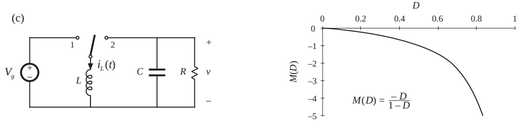
Buck



Boost



Buck-boost



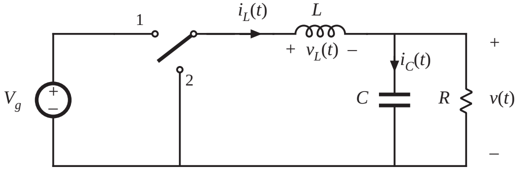
Objectives of this chapter

- Develop techniques for easily determining output voltage of an arbitrary converter circuit
- Derive the principles of *inductor volt-second balance* and *capacitor charge (amp-second) balance*
- Introduce the key *small ripple approximation*
- Develop simple methods for selecting filter element values
- Illustrate via examples

2.2. Inductor volt-second balance, capacitor charge balance, and the small ripple approximation

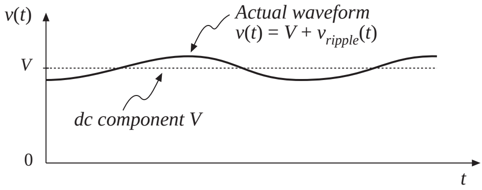
Actual output voltage waveform, buck converter

Buck converter containing practical low-pass filter



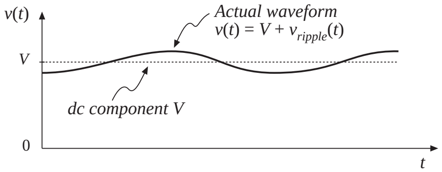
Actual output voltage waveform

$v(t) = V + v_{ripple}(t)$



The small ripple approximation

$$v(t) = V + v_{ripple}(t)$$

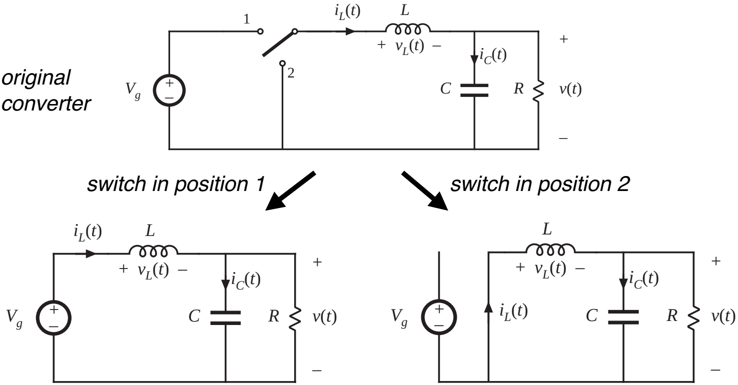


In a well-designed converter, the output voltage ripple is small. Hence, the waveforms can be easily determined by ignoring the ripple:

$$\left\| v_{ripple} \right\| \ll V$$

$$v(t) \approx V$$

Buck converter analysis: inductor current waveform



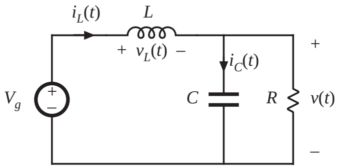
Inductor voltage and current
Subinterval 1: switch in position 1

Inductor voltage

$$v_L = V_g - v(t)$$

Small ripple approximation:

$$v_L \approx V_g - V$$



Knowing the inductor voltage, we can now find the inductor current via

$$v_L(t) = L \frac{di_L(t)}{dt}$$

Solve for the slope:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} \approx \frac{V_g - V}{L}$$

$\Rightarrow$ *The inductor current changes with an essentially constant slope*

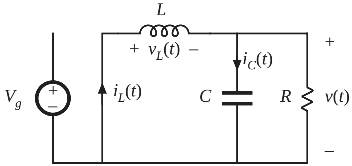
Inductor voltage and current
Subinterval 2: switch in position 2

Inductor voltage

$$v_L(t) = -v(t)$$

Small ripple approximation:

$$v_L(t) \approx -V$$



Knowing the inductor voltage, we can again find the inductor current via

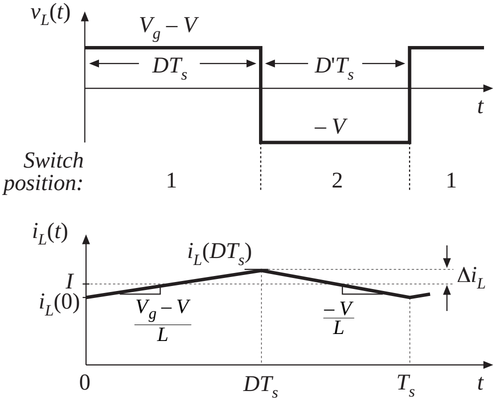
$$v_L(t) = L\,\frac{di_L(t)}{dt}$$

Solve for the slope:

$$\frac{di_L(t)}{dt} \approx -\frac{V}{L}$$

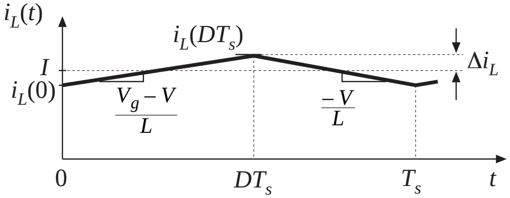
$\Rightarrow$ *The inductor current changes with an essentially constant slope*

Inductor voltage and current waveforms



$$v_L(t) = L\,\frac{di_L(t)}{dt}$$

Determination of inductor current ripple magnitude

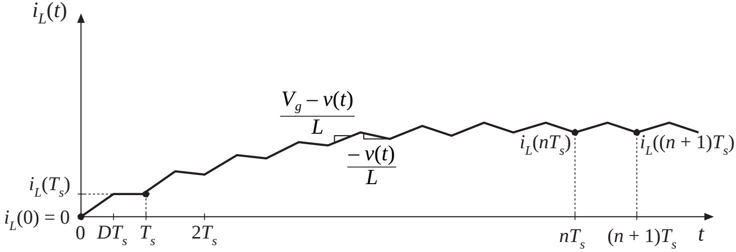


$$(\textit{change in } i_L) = (\textit{slope})(\textit{length of subinterval})$$

$$\left(2\Delta i_L\right) = \left(\frac{V_g - V}{L}\right)\left(DT_s\right)$$

$$\Rightarrow \qquad \Delta i_L = \frac{V_g - V}{2L} DT_s \qquad\qquad L = \frac{V_g - V}{2\Delta i_L} DT_s$$

Inductor current waveform during turn-on transient



When the converter operates in equilibrium:

$$i_L((n+1)T_s) = i_L(nT_s)$$

The principle of inductor volt-second balance: Derivation

Inductor defining relation:

$$v_L(t) = L\,\frac{di_L(t)}{dt}$$

Integrate over one complete switching period:

$$i_L(T_s) - i_L(0) = \frac{1}{L}\int_0^{T_s} v_L(t)\,dt$$

In periodic steady state, the net change in inductor current is zero:

$$0 = \int_0^{T_s} v_L(t)\,dt$$

Hence, the total area (or volt-seconds) under the inductor voltage waveform is zero whenever the converter operates in steady state.

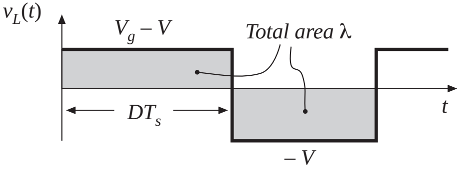
An equivalent form:

$$0 = \frac{1}{T_s}\int_0^{T_s} v_L(t)\,dt = \left\langle v_L \right\rangle$$

The average inductor voltage is zero in steady state.

Inductor volt-second balance: Buck converter example

Inductor voltage waveform, previously derived:



Integral of voltage waveform is area of rectangles:

$$\lambda = \int_0^{T_s} v_L(t)\, dt = (V_g - V)(DT_s) + (-V)(D'T_s)$$

Average voltage is

$$\langle v_L \rangle = \frac{\lambda}{T_s} = D(V_g - V) + D'(-V)$$

Equate to zero and solve for *V:*

$$0 = DV_g - (D + D')V = DV_g - V \qquad \Rightarrow \qquad V = DV_g$$

The principle of capacitor charge balance: Derivation

Capacitor defining relation:

$$i_C(t) = C\,\frac{dv_C(t)}{dt}$$

Integrate over one complete switching period:

$$v_C(T_s) - v_C(0) = \frac{1}{C}\int_0^{T_s} i_C(t)\,dt$$

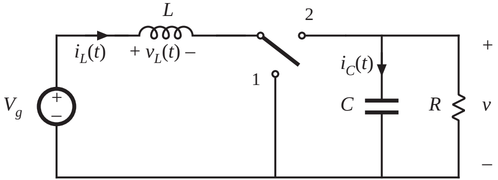
In periodic steady state, the net change in capacitor voltage is zero:

$$0 = \frac{1}{T_s}\int_0^{T_s} i_C(t)\,dt = \left\langle i_C \right\rangle$$

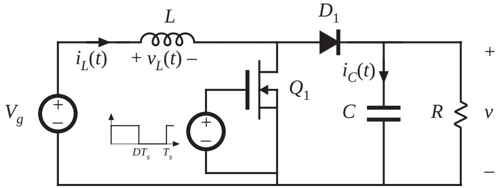
Hence, the total area (or charge) under the capacitor current waveform is zero whenever the converter operates in steady state. The average capacitor current is then zero.

2.3 Boost converter example

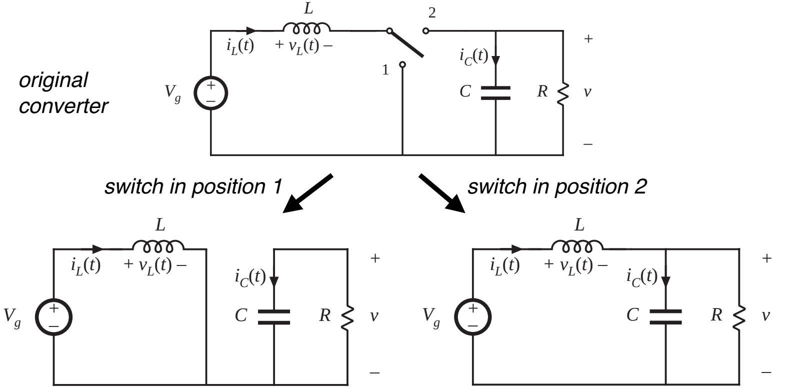
Boost converter with ideal switch



Realization using power MOSFET and diode



Boost converter analysis



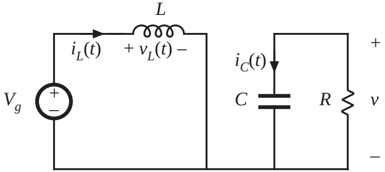
Subinterval 1: switch in position 1

Inductor voltage and capacitor current

$$v_L = V_g$$
$$i_C = -v\ /\ R$$

Small ripple approximation:

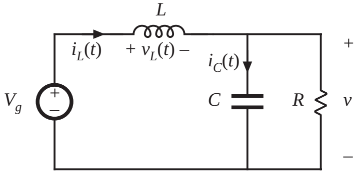
$$v_L = V_g$$
$$i_C = -V\ /\ R$$



Subinterval 2: switch in position 2

Inductor voltage and capacitor current

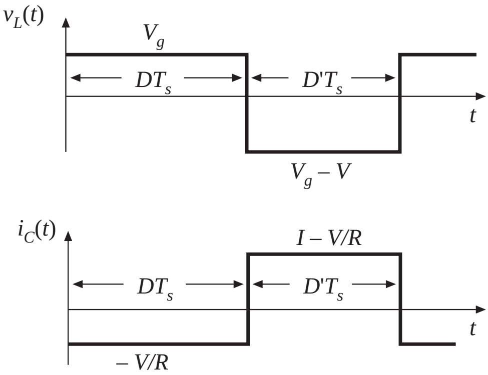
$$v_L = V_g - v$$
$$i_C = i_L - v / R$$



Small ripple approximation:

$$v_L = V_g - V$$
$$i_C = I - V / R$$

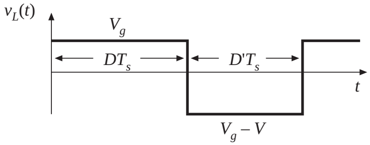
Inductor voltage and capacitor current waveforms



Inductor volt-second balance

Net volt-seconds applied to inductor over one switching period:

$$\int_0^{T_s} v_L(t)\, dt = (V_g)\, DT_s + (V_g - V)\, D'T_s$$



Equate to zero and collect terms:

$$V_g\,(D + D') - V\,D' = 0$$

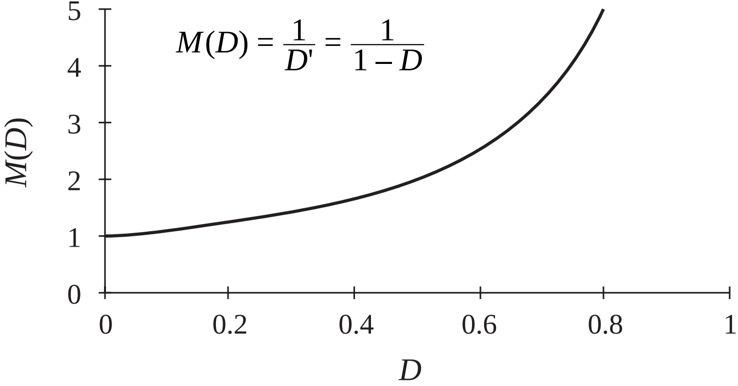
Solve for V:

$$V = \frac{V_g}{D'}$$

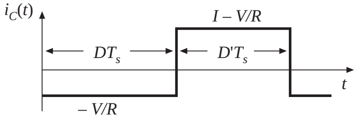
The voltage conversion ratio is therefore

$$M(D) = \frac{V}{V_g} = \frac{1}{D'} = \frac{1}{1 - D}$$

Conversion ratio *M(D)* of the boost converter



Determination of inductor current dc component



Capacitor charge balance:

$$\int_0^{T_s} i_C(t)\, dt = (-\frac{V}{R})\, DT_s + (I - \frac{V}{R})\, D'T_s$$

Collect terms and equate to zero:

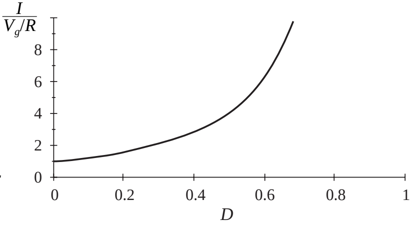
$$-\frac{V}{R}(D + D') + I\, D' = 0$$

Solve for I:

$$I = \frac{V}{D'\, R}$$

Eliminate V to express in terms of V_g:

$$I = \frac{V_g}{D'^2\, R}$$



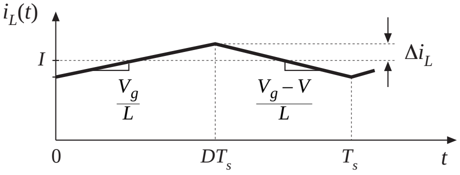
Determination of inductor current ripple

Inductor current slope during subinterval 1:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g}{L}$$

Inductor current slope during subinterval 2:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g - V}{L}$$



Change in inductor current during subinterval 1 is *(slope) (length of subinterval):*

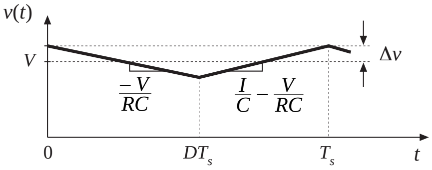
$$2\Delta i_L = \frac{V_g}{L} DT_s$$

Solve for peak ripple:

$$\Delta i_L = \frac{V_g}{2L} DT_s$$

- Choose *L* such that desired ripple magnitude is obtained

Determination of capacitor voltage ripple



Capacitor voltage slope during subinterval 1:

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = \frac{-V}{RC}$$

Capacitor voltage slope during subinterval 2:

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = \frac{I}{C} - \frac{V}{RC}$$

Change in capacitor voltage during subinterval 1 is *(slope) (length of subinterval):*

$$-2\Delta v = \frac{-V}{RC} DT_s$$

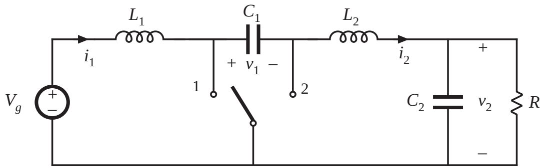
Solve for peak ripple:

$$\Delta v = \frac{V}{2RC} DT_s$$

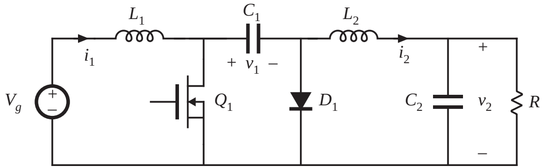
- Choose *C* such that desired voltage ripple magnitude is obtained
- In practice, capacitor *equivalent series resistance* (esr) leads to increased voltage ripple

2.4 Cuk converter example

Cuk converter, with ideal switch



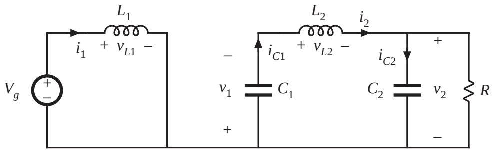
Cuk converter: practical realization using MOSFET and diode



Cuk converter circuit
with switch in positions 1 and 2

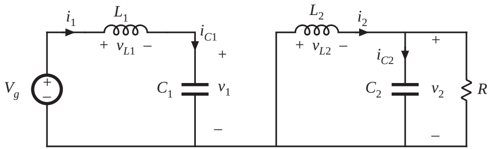
Switch in position 1: MOSFET conducts

Capacitor C_1 releases energy to output



Switch in position 2: diode conducts

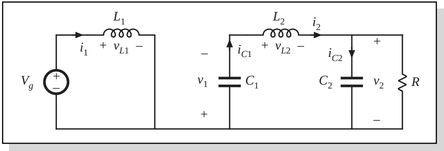
Capacitor C_1 is charged from input



Waveforms during subinterval 1
MOSFET conduction interval

Inductor voltages and capacitor currents:

$$v_{L1} = V_g$$
$$v_{L2} = -v_1 - v_2$$
$$i_{C1} = i_2$$
$$i_{C2} = i_2 - \frac{v_2}{R}$$



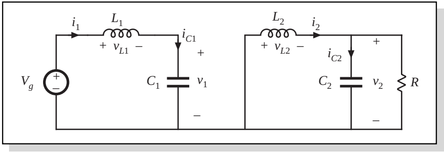
Small ripple approximation for subinterval 1:

$$v_{L1} = V_g$$
$$v_{L2} = -V_1 - V_2$$
$$i_{C1} = I_2$$
$$i_{C2} = I_2 - \frac{V_2}{R}$$

Waveforms during subinterval 2
Diode conduction interval

Inductor voltages and capacitor currents:

$$v_{L1} = V_g - v_1$$
$$v_{L2} = - v_2$$
$$i_{C1} = i_1$$
$$i_{C2} = i_2 - \frac{v_2}{R}$$



Small ripple approximation for subinterval 2:

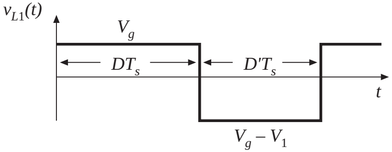
$$v_{L1} = V_g - V_1$$
$$v_{L2} = - V_2$$
$$i_{C1} = I_1$$
$$i_{C2} = I_2 - \frac{V_2}{R}$$

Equate average values to zero

The principles of inductor volt-second and capacitor charge balance state that the average values of the periodic inductor voltage and capacitor current waveforms are zero, when the converter operates in steady state. Hence, to determine the steady-state conditions in the converter, let us sketch the inductor voltage and capacitor current waveforms, and equate their average values to zero.

Waveforms:

Inductor voltage $v_{L1}(t)$

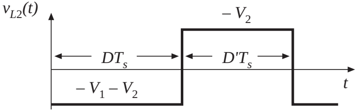


Volt-second balance on L_1:

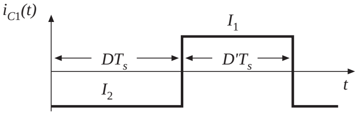
$$\left\langle v_{L1} \right\rangle = DV_g + D'(V_g - V_1) = 0$$

Equate average values to zero

Inductor L_2 *voltage*



Capacitor C_1 *current*

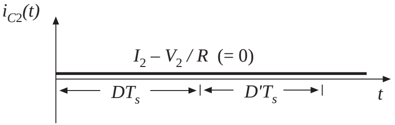


Average the waveforms:

$$\langle v_{L2} \rangle = D(-V_1 - V_2) + D'(-V_2) = 0$$
$$\langle i_{C1} \rangle = DI_2 + D'I_1 = 0$$

Equate average values to zero

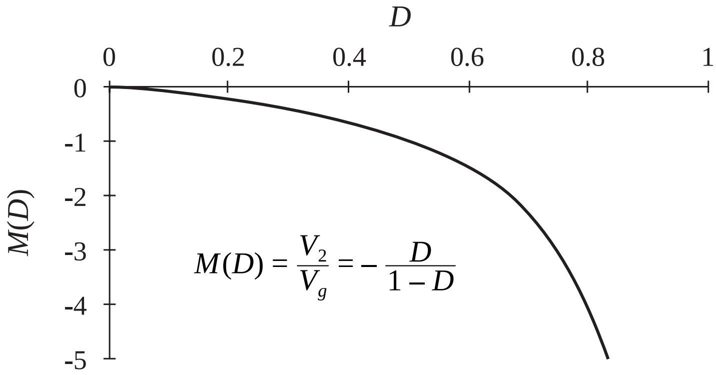
Capacitor current $i_{C2}(t)$ waveform



$$\langle i_{C2} \rangle = I_2 - \frac{V_2}{R} = 0$$

Note: during both subintervals, the capacitor current i_{C2} is equal to the difference between the inductor current i_2 and the load current V_2/R. When ripple is neglected, i_{C2} is constant and equal to zero.

Cuk converter conversion ratio $M = V / V_g$



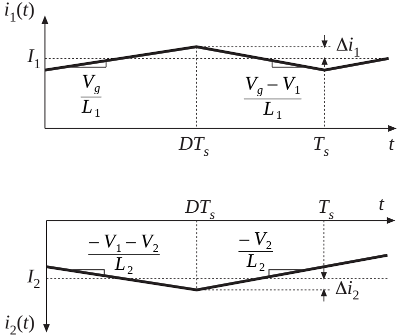
Inductor current waveforms

Interval 1 slopes, using small ripple approximation:

$$\frac{di_1(t)}{dt} = \frac{v_{L1}(t)}{L_1} = \frac{V_g}{L_1}$$
$$\frac{di_2(t)}{dt} = \frac{v_{L2}(t)}{L_2} = \frac{-V_1 - V_2}{L_2}$$

Interval 2 slopes:

$$\frac{di_1(t)}{dt} = \frac{v_{L1}(t)}{L_1} = \frac{V_g - V_1}{L_1}$$
$$\frac{di_2(t)}{dt} = \frac{v_{L2}(t)}{L_2} = \frac{-V_2}{L_2}$$



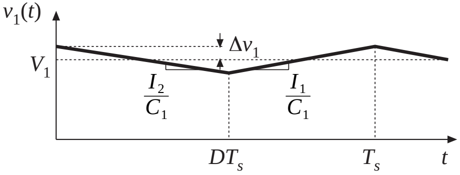
Capacitor C_1 waveform

Subinterval 1:

$$\frac{dv_1(t)}{dt} = \frac{i_{C1}(t)}{C_1} = \frac{I_2}{C_1}$$

Subinterval 2:

$$\frac{dv_1(t)}{dt} = \frac{i_{C1}(t)}{C_1} = \frac{I_1}{C_1}$$



Ripple magnitudes

Analysis results

$$\Delta i_1 = \frac{V_g D T_s}{2L_1}$$

$$\Delta i_2 = \frac{V_1 + V_2}{2L_2} D T_s$$

$$\Delta v_1 = \frac{-I_2 D T_s}{2C_1}$$

Use dc converter solution to simplify:

$$\Delta i_1 = \frac{V_g D T_s}{2L_1}$$

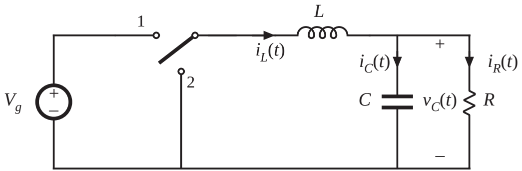
$$\Delta i_2 = \frac{V_g D T_s}{2L_2}$$

$$\Delta v_1 = \frac{V_g D^2 T_s}{2D' R C_1}$$

Q: How large is the output voltage ripple?

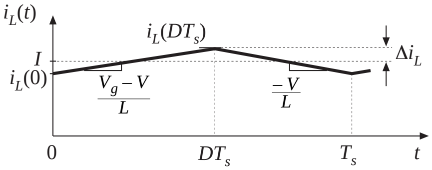
2.5 Estimating ripple in converters containing two-pole low-pass filters

Buck converter example: Determine output voltage ripple



Inductor current waveform.

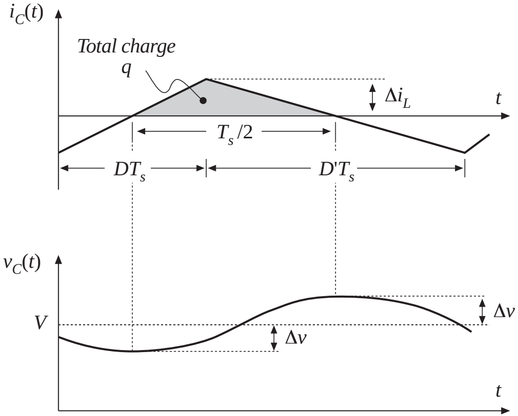
What is the capacitor current?



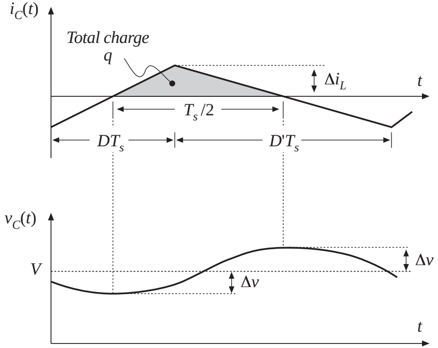
Capacitor current and voltage, buck example

Must not neglect inductor current ripple!

If the capacitor voltage ripple is small, then essentially all of the ac component of inductor current flows through the capacitor.



Estimating capacitor voltage ripple Δv

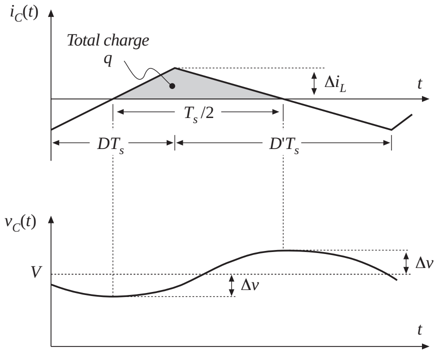


Current $i_C(t)$ is positive for half of the switching period. This positive current causes the capacitor voltage $v_C(t)$ to increase between its minimum and maximum extrema. During this time, the total charge q is deposited on the capacitor plates, where

$$q = C\,(2\Delta v)$$

(*change in charge*) = C (*change in voltage*)

Estimating capacitor voltage ripple Δv



The total charge q is the area of the triangle, as shown:

$$q = \frac{1}{2}\Delta i_L \frac{T_s}{2}$$

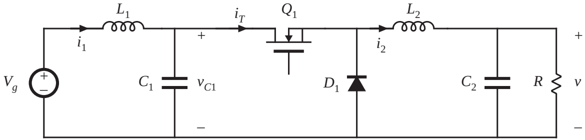
Eliminate q and solve for Δv:

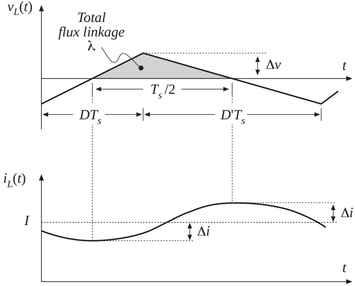
$$\Delta v = \frac{\Delta i_L\, T_s}{8\, C}$$

Note: in practice, capacitor equivalent series resistance (esr) further increases Δv.

Inductor current ripple in two-pole filters

Example:
problem 2.9





can use similar arguments, with

$$\lambda = L\,(2\Delta i)$$

λ = inductor flux linkages

= inductor volt-seconds

Inductor volt-second balance, capacitor charge balance, the fast way

The inductor volt-second balance and capacitor charge balance can be applied systematically as previously explained yielding to several equations to be solved. By inspecting the circuit it is possible to deduce some relationship in a faster way.
Note: the underlying inductor volt-second balance and capacitor charge balance principles are still applied.

- Replace inductors by short-circuits to deduce average voltages across capacitors.
- Replace capacitors by open-circuits to deduce average inductors and switches currents.

Example: CUK converter

2.6 Summary of Key Points

1. The dc component of a converter waveform is given by its average value, or the integral over one switching period, divided by the switching period. Solution of a dc-dc converter to find its dc, or steady-state, voltages and currents therefore involves averaging the waveforms.
2. The linear ripple approximation greatly simplifies the analysis. In a well-designed converter, the switching ripples in the inductor currents and capacitor voltages are small compared to the respective dc components, and can be neglected.
3. The principle of inductor volt-second balance allows determination of the dc voltage components in any switching converter. In steady-state, the average voltage applied to an inductor must be zero.

Summary of Chapter 2

4. The principle of capacitor charge balance allows determination of the dc components of the inductor currents in a switching converter. In steady-state, the average current applied to a capacitor must be zero.
5. By knowledge of the slopes of the inductor current and capacitor voltage waveforms, the ac switching ripple magnitudes may be computed. Inductance and capacitance values can then be chosen to obtain desired ripple magnitudes.
6. In converters containing multiple-pole filters, continuous (nonpulsating) voltages and currents are applied to one or more of the inductors or capacitors. Computation of the ac switching ripple in these elements can be done using capacitor charge and/or inductor flux-linkage arguments, without use of the small-ripple approximation.
7. Converters capable of increasing (boost), decreasing (buck), and inverting the voltage polarity (buck-boost and Cuk) have been described. Converter circuits are explored more fully in a later chapter.

Chapter 3: Steady-State Equivalent Circuit Modeling, Losses, and Efficiency

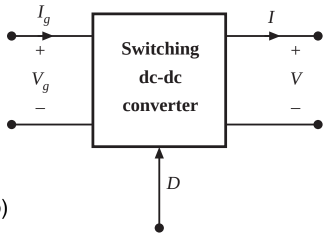
- 3.1 The dc transformer model
- 3.2 Inclusion of inductor copper loss
- 3.3 Construction of equivalent circuit model
- 3.4 How to obtain the input port of the model
- 3.5 Example: inclusion of semiconductor conduction losses in the boost converter model
- 3.6 Summary of key points

3.1. The dc transformer model

Basic equations of an ideal dc-dc converter:

$$P_{in} = P_{out} \qquad (\eta = 100\%)$$
$$V_g I_g = V I$$

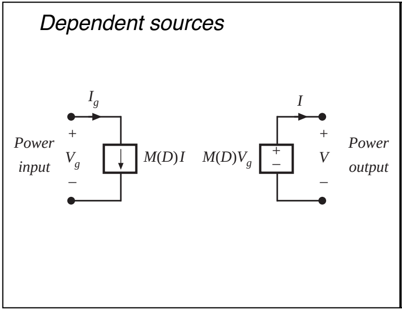
$$V = M(D) V_g \qquad \text{(ideal conversion ratio)}$$
$$I_g = M(D) I$$

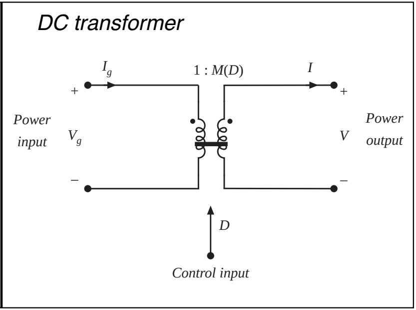


These equations are valid in steady-state. During transients, energy storage within filter elements may cause $P_{in} \neq P_{out}$

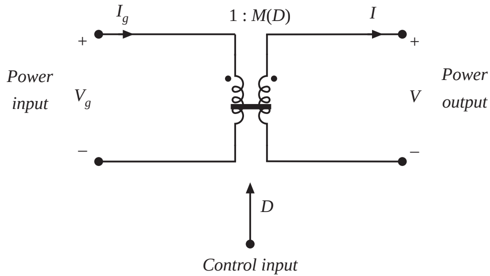
Equivalent circuits corresponding to ideal dc-dc converter equations

$$P_{in} = P_{out} \qquad V_g I_g = V I \qquad V = M(D) V_g \qquad I_g = M(D) I$$





The DC transformer model



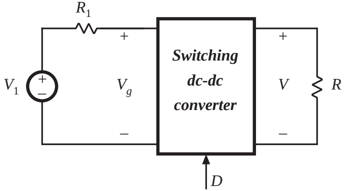
Models basic properties of ideal dc-dc converter:

- conversion of dc voltages and currents, ideally with 100% efficiency
- conversion ratio M controllable via duty cycle

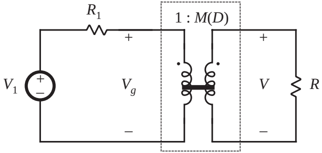
- Solid line denotes ideal transformer model, capable of passing dc voltages and currents
- Time-invariant model (no switching) which can be solved to find dc components of converter waveforms

Example: use of the DC transformer model

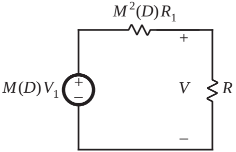
1. Original system



2. Insert dc transformer model



3. Push source through transformer



4. Solve circuit

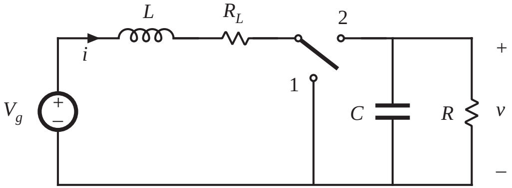
$$V = M(D)\, V_1 \, \frac{R}{R + M^2(D)\, R_1}$$

3.2. Inclusion of inductor copper loss

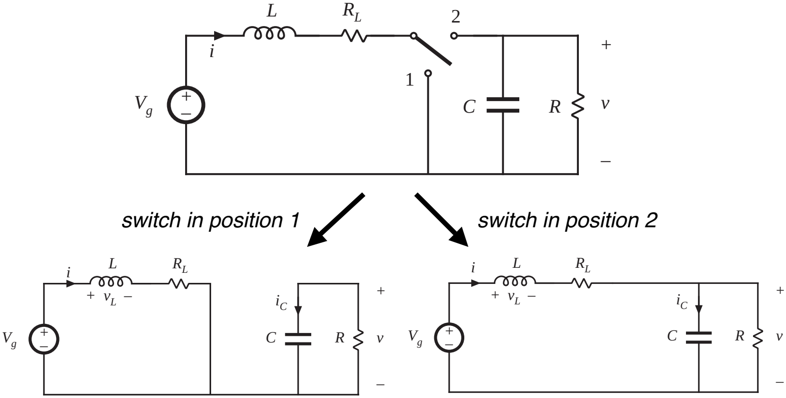
Dc transformer model can be extended, to include converter nonidealities.

Example: inductor copper loss (resistance of winding):

Insert this inductor model into boost converter circuit:



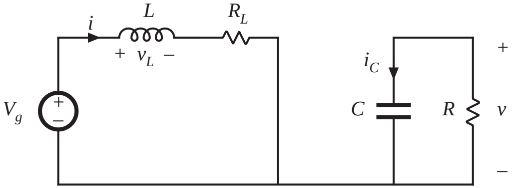
Analysis of nonideal boost converter



Circuit equations, switch in position 1

Inductor current and capacitor voltage:

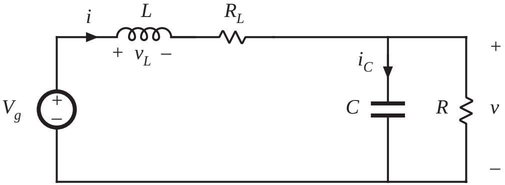
$$v_L(t) = V_g - i(t)\, R_L$$
$$i_C(t) = -v(t) / R$$



Small ripple approximation:

$$v_L(t) = V_g - I\, R_L$$
$$i_C(t) = -V / R$$

Circuit equations, switch in position 2



$$v_L(t) = V_g - i(t)\,R_L - v(t) \approx V_g - I\,R_L - V$$
$$i_C(t) = i(t) - v(t)\,/\,R \approx I - V\,/\,R$$

Inductor voltage and capacitor current waveforms

Average inductor voltage:

$$\left\langle v_L(t) \right\rangle = \frac{1}{T_s}\int_0^{T_s} v_L(t)dt$$
$$= D(V_g - I\,R_L) + D'(V_g - I\,R_L - V)$$

Inductor volt-second balance:

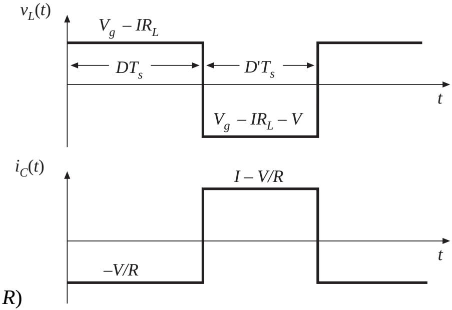
$$0 = V_g - I\,R_L - D'V$$

Average capacitor current:

$$\left\langle i_C(t) \right\rangle = D\,(-V/R) + D'\,(I - V/R)$$

Capacitor charge balance:

$$0 = D'I - V/R$$



Solution for output voltage

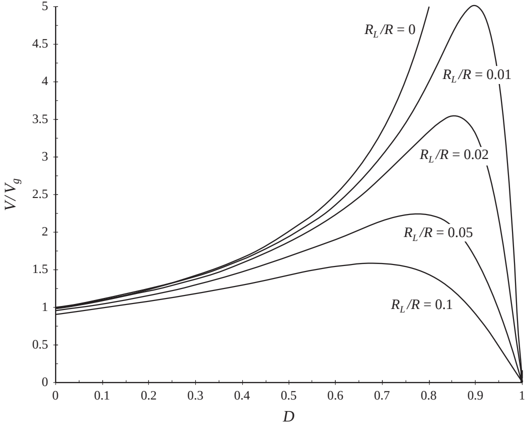
We now have two equations and two unknowns:

$$0 = V_g - I\,R_L - D'V$$

$$0 = D'I - V\,/\,R$$

Eliminate I and solve for V:

$$\frac{V}{V_g} = \frac{1}{D'}\,\frac{1}{(1 + R_L\,/\,D'^2 R)}$$



3.3. Construction of equivalent circuit model

Results of previous section (derived via inductor volt-sec balance and capacitor charge balance):

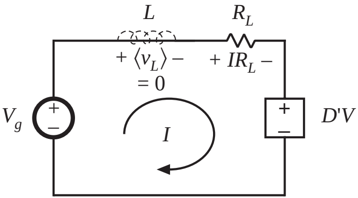
$$\langle v_L \rangle = 0 = V_g - I\,R_L - D'V$$
$$\langle i_C \rangle = 0 = D'I - V/R$$

View these as loop and node equations of the equivalent circuit. Reconstruct an equivalent circuit satisfying these equations

Inductor voltage equation

$$\langle v_L \rangle = 0 = V_g - I\,R_L - D'V$$

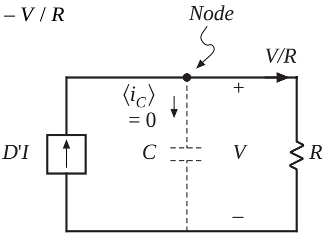
- Derived via Kirchhoff's voltage law, to find the inductor voltage during each subinterval
- Average inductor voltage then set to zero
- This is a loop equation: the dc components of voltage around a loop containing the inductor sum to zero



- IR_L term: voltage across resistor of value R_L having current I
- $D'V$ term: for now, leave as dependent source

Capacitor current equation

$$\langle i_C \rangle = 0 = D'I - V / R$$

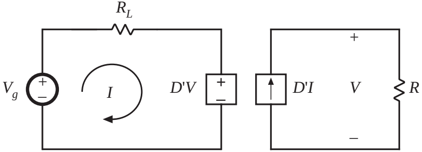


- Derived via Kirchoff's current law, to find the capacitor current during each subinterval
- Average capacitor current then set to zero
- This is a node equation: the dc components of current flowing into a node connected to the capacitor sum to zero

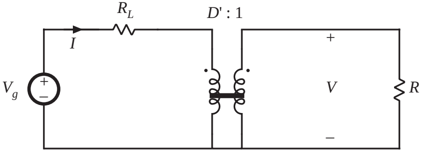
- V/R term: current through load resistor of value R having voltage V
- $D'I$ term: for now, leave as dependent source

Complete equivalent circuit

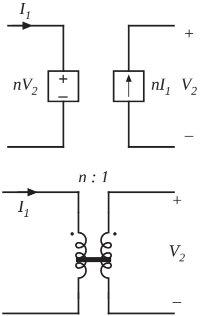
The two circuits, drawn together:



The dependent sources are equivalent to a D' : 1 transformer:



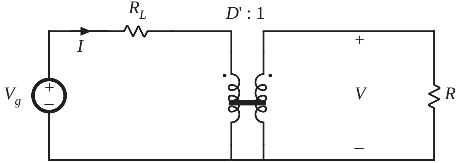
Dependent sources and transformers



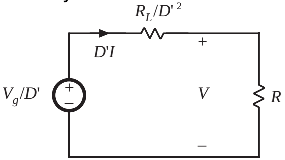
- *sources have same coefficient*
- *reciprocal voltage/current dependence*

Solution of equivalent circuit

Converter equivalent circuit



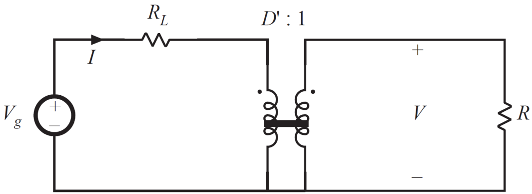
Refer all elements to transformer secondary:



Solution for output voltage using voltage divider formula:

$$V = \frac{V_g}{D'} \frac{R}{R + \frac{R_L}{D'^2}} = \frac{V_g}{D'} \frac{1}{1 + \frac{R_L}{D'^2\,R}}$$

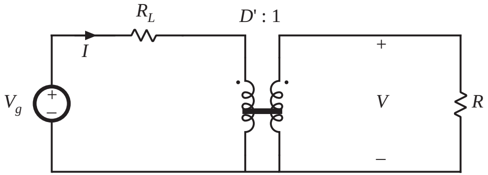
Solution for input (inductor) current



$$I = \frac{V_g}{D'^2 R + R_L} = \frac{V_g}{D'^2 R} \frac{1}{1 + \frac{R_L}{D'^2 R}}$$

Solution for converter efficiency

$$P_{in} = (V_g)\,(I)$$



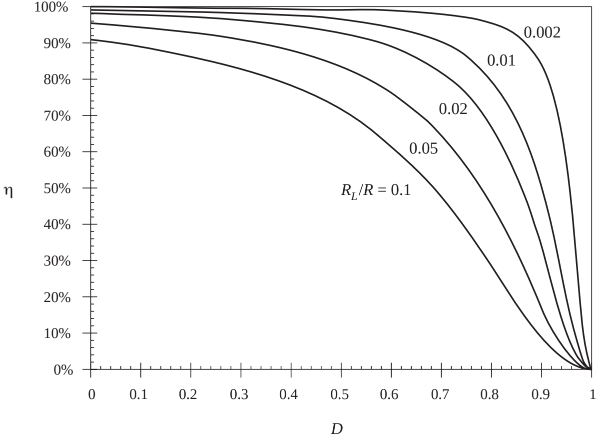
$$P_{out} = (V)\,(D'I)$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{(V)\,(D'I)}{(V_g)\,(I)} = \frac{V}{V_g}\,D'$$

$$\eta = \frac{1}{1 + \dfrac{R_L}{D'^2\,R}}$$

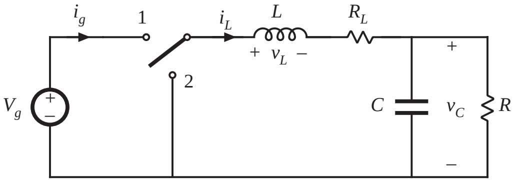
Efficiency, for various values of R_L

$$\eta = \frac{1}{1 + \frac{R_L}{D'^2 R}}$$



3.4. How to obtain the input port of the model

Buck converter example —use procedure of previous section to derive equivalent circuit

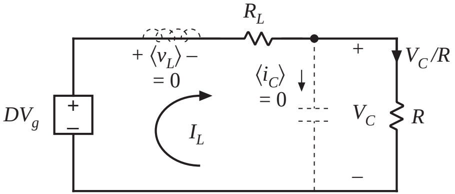


Average inductor voltage and capacitor current:

$$\langle v_L \rangle = 0 = DV_g - I_L R_L - V_C \qquad \langle i_C \rangle = 0 = I_L - V_C/R$$

Construct equivalent circuit as usual

$$\langle v_L \rangle = 0 = DV_g - I_L R_L - V_C \qquad \langle i_C \rangle = 0 = I_L - V_C/R$$

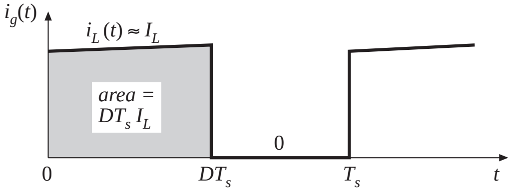


What happened to the transformer?

- Need another equation

Modeling the converter input port

Input current waveform $i_g(t)$:

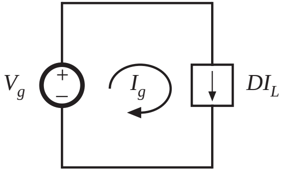


Dc component (average value) of $i_g(t)$ is

$$I_g = \frac{1}{T_s} \int_0^{T_s} i_g(t)\, dt = DI_L$$

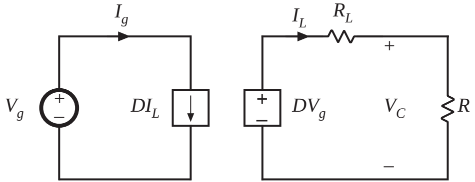
Input port equivalent circuit

$$I_g = \frac{1}{T_s} \int_0^{T_s} i_g(t)\, dt = DI_L$$

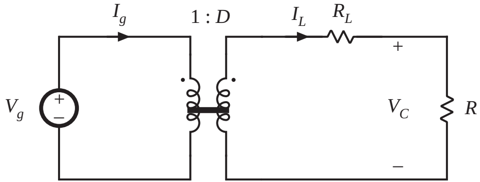


Complete equivalent circuit, buck converter

Input and output port equivalent circuits, drawn together:

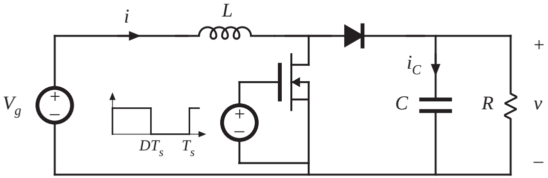


Replace dependent sources with equivalent dc transformer:



3.5. Example: inclusion of semiconductor conduction losses in the boost converter model

Boost converter example



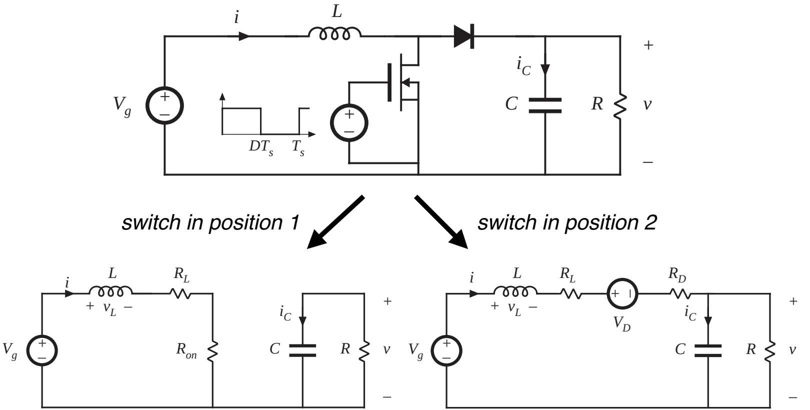
Models of on-state semiconductor devices:

MOSFET: on-resistance R_{on}

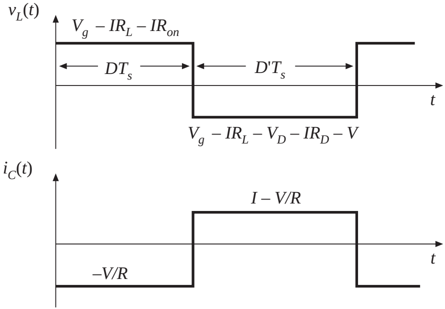
Diode: constant forward voltage V_D plus on-resistance R_D

Insert these models into subinterval circuits

Boost converter example: circuits during subintervals 1 and 2



Average inductor voltage and capacitor current

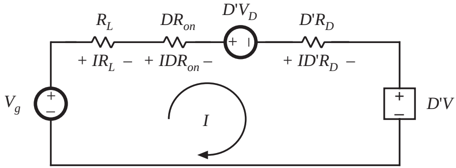


$$\langle v_L \rangle = D(V_g - IR_L - IR_{on}) + D'(V_g - IR_L - V_D - IR_D - V) = 0$$

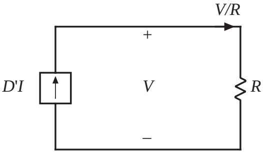
$$\langle i_C \rangle = D(-V/R) + D'(I - V/R) = 0$$

Construction of equivalent circuits

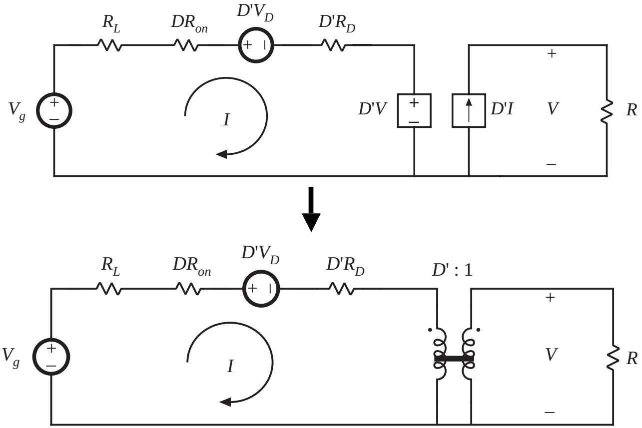
$$V_g - IR_L - IDR_{on} - D'V_D - ID'R_D - D'V = 0$$



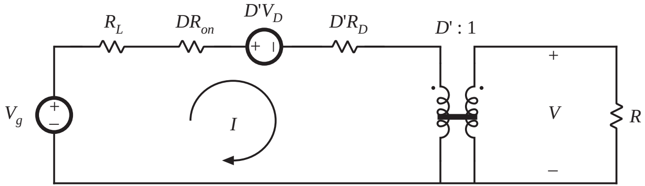
$$D'I - V/R = 0$$



Complete equivalent circuit



Solution for output voltage



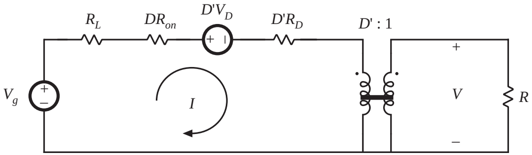
$$V = \left(\frac{1}{D'}\right)\left(V_g - D'V_D\right)\left(\frac{D'^2 R}{D'^2 R + R_L + DR_{on} + D'R_D}\right)$$

$$\frac{V}{V_g} = \left(\frac{1}{D'}\right)\left(1 - \frac{D'V_D}{V_g}\right)\left(\frac{1}{1 + \dfrac{R_L + DR_{on} + D'R_D}{D'^2 R}}\right)$$

Solution for converter efficiency

$$P_{in} = (V_g)\,(I)$$

$$P_{out} = (V)\,(D'I)$$



$$\eta = D' \frac{V}{V_g} = \frac{\left(1 - \dfrac{D'V_D}{V_g}\right)}{\left(1 + \dfrac{R_L + DR_{on} + D'R_D}{D'^2 R}\right)}$$

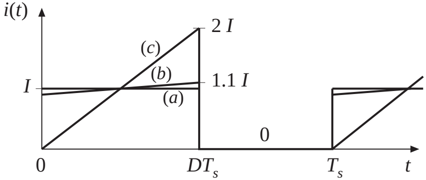
Conditions for high efficiency:

$$V_g/D' \gg V_D$$
$$D'^2 R \gg R_L + DR_{on} + D'R_D$$

Accuracy of the averaged equivalent circuit in prediction of losses

- Model uses average currents and voltages
- To correctly predict power loss in a resistor, use rms values
- Result is the same, provided ripple is small

MOSFET current waveforms, for various ripple magnitudes:



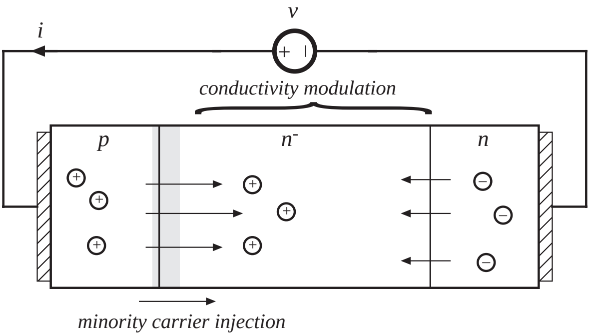
Inductor current ripple	*MOSFET rms current*	*Average power loss in R_{on}*
(a) $\Delta i = 0$	$I\sqrt{D}$	$D\,I^2\,R_{on}$
(b) $\Delta i = 0.1\,I$	$(1.00167)\,I\sqrt{D}$	$(1.0033)\,D\,I^2\,R_{on}$
(c) $\Delta i = I$	$(1.155)\,I\sqrt{D}$	$(1.3333)\,D\,I^2\,R_{on}$

Summary of chapter 3

1. The dc transformer model represents the primary functions of any dc-dc converter: transformation of dc voltage and current levels, ideally with 100% efficiency, and control of the conversion ratio M via the duty cycle D. This model can be easily manipulated and solved using familiar techniques of conventional circuit analysis.
2. The model can be refined to account for loss elements such as inductor winding resistance and semiconductor on-resistances and forward voltage drops. The refined model predicts the voltages, currents, and efficiency of practical nonideal converters.
3. In general, the dc equivalent circuit for a converter can be derived from the inductor volt-second balance and capacitor charge balance equations. Equivalent circuits are constructed whose loop and node equations coincide with the volt-second and charge balance equations. In converters having a pulsating input current, an additional equation is needed to model the converter input port; this equation may be obtained by averaging the converter input current.

- Diode
  - Physics of the diode: charge-controlled behavior
  - Switching losses
  - Ringing induced by diode stored charge
  - Examples of diodes
- MOSFET
  - Physics of the MOSFET
  - Static characteristics
  - Output capacitance
  - Hard switching losses
  - Examples of MOSFET
- Switch selection: controlled switch or diode?
- Other power semi-conductors

Forward-biased power diode



Charge-controlled behavior of the diode

The diode equation:

$$q(t) = Q_0\left(e^{\lambda v(t)} - 1\right)$$

Charge control equation:

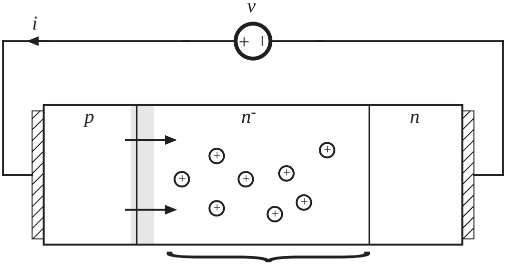
$$\frac{dq(t)}{dt} = i(t) - \frac{q(t)}{\tau_L}$$

With:

λ= 1/(26 mV) at 300 K

τ_L = minority carrier lifetime

(above equations don't include current that charges depletion region capacitance)



Total stored minority charge q

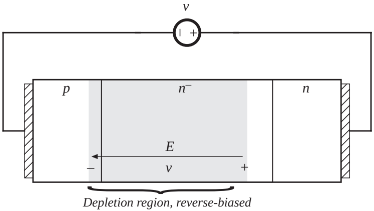
In equilibrium: $dq/dt = 0$, and hence

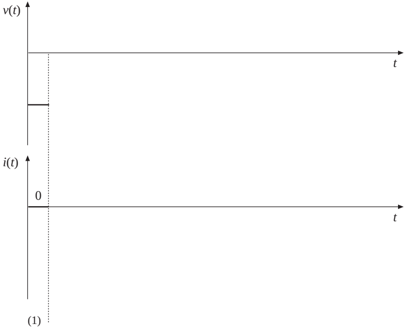
$$i(t) = \frac{q(t)}{\tau_L} = \frac{Q_0}{\tau_L}\left(e^{\lambda v(t)} - 1\right) = I_0\left(e^{\lambda v(t)} - 1\right)$$

Charge-control in the diode: Discussion

- The familiar i–v curve of the diode is an equilibrium relationship that can be violated during transient conditions
- During the turn-on and turn-off switching transients, the current deviates substantially from the equilibrium i–v curve, because of change in the stored charge and change in the charge within the reverse-bias depletion region
- Under forward-biased conditions, the stored minority charge causes "conductivity modulation" of the resistance of the lightly-doped n^- region, reducing the device on-resistance

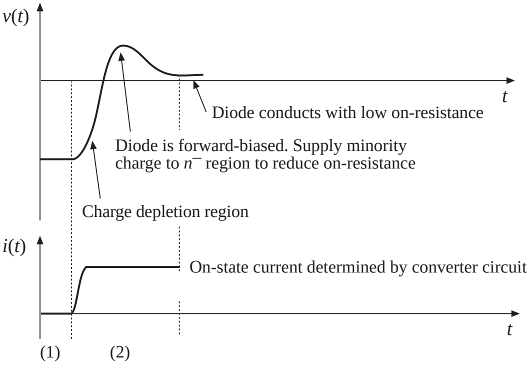
Diode in OFF state: reversed-biased, blocking voltage





- Diode is reverse-biased
- No stored minority charge: $q = 0$
- Depletion region blocks applied reverse voltage; charge is stored in capacitance of depletion region

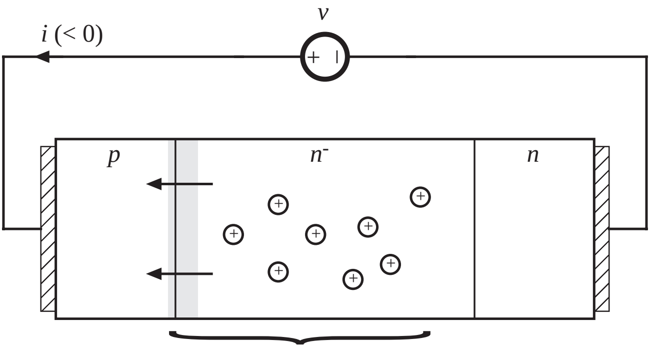
Turn-on transient



The current $i(t)$ is determined by the converter circuit. This current supplies:

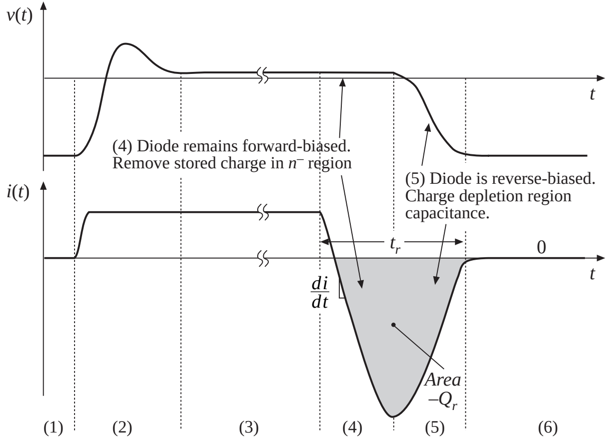
- charge to increase voltage across depletion region
- charge needed to support the on-state current
- charge to reduce on-resistance of n^{-} region

Turn-off transient



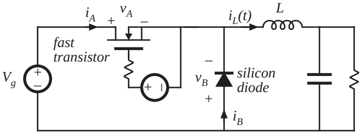
Removal of stored minority charge q

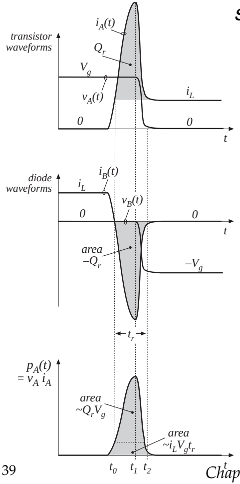
Diode turn-off transient
continued



The diode switching transients induce switching loss in the transistor

see Section 4.3.2





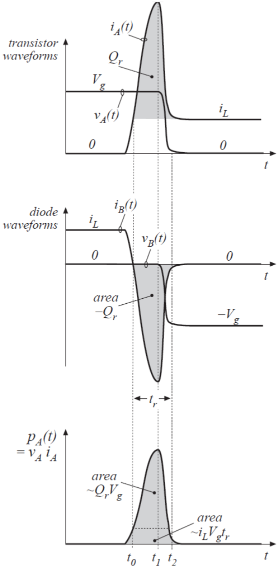
- Diode recovered stored charge Q_r flows through transistor during transistor turn-on transition, inducing switching loss
- Q_r depends on diode on-state forward current, and on the rate-of-change of diode current during diode turn-off transition

Diode reverse recovery: transistor induced losses

Losses are induced in the transistor because the diode reverse voltage takes time to establish.
Assuming abrupt recovery, losses are essentially present in the transistor:

$$W_T = \int_{t_0 \to t_1} v_A(t) i_A(t) dt$$
$$\approx \int_{t_0 \to t_1} V_g (i_L - i_B(t)) dt$$
$$= V_g i_L (t_1 - t_0) + V_g Q_r.$$

Excerpt of [1]:



Soft-recovery diode:

$(t_2 - t_1) >> (t_1 - t_0)$

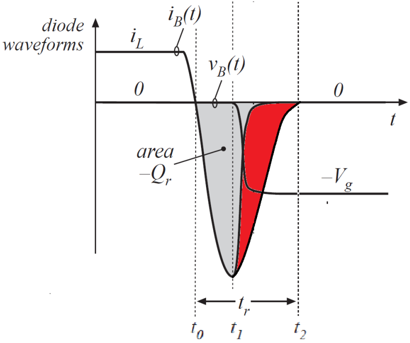
Abrupt-recovery diode:

$(t_2 - t_1) << (t_1 - t_0)$

Once the transistor is closed, the diode sees the full voltage and experiences a non negligible trailing current (soft recovery case):

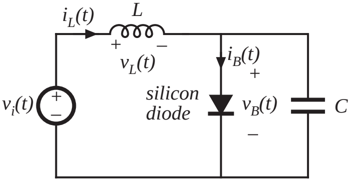
$$
\begin{aligned}
W_D &= \int_{t_1 \to t_2} v_B(t) i_B(t) dt \\
&\approx \int_{t_1 \to t_2} -V_g \cdot i_B(t) dt \\
&= -V_g \int_{t_1 \to t_2} i_B(t) dt \\
&= V_g Q_{red}.
\end{aligned}
$$

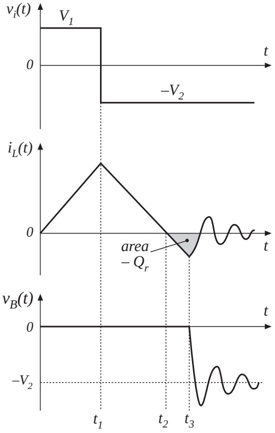
Modified figure of [1]:



Ringing induced by diode stored charge

see Section 4.3.3





- Diode is forward-biased while $i_L(t) > 0$
- Negative inductor current removes diode stored charge Q_r
- When diode becomes reverse-biased, negative inductor current flows through capacitor C.
- Ringing of L-C network is damped by parasitic losses. Ringing energy is lost.

Energy associated with ringing

Recovered charge is $Q_r = -\int_{t_2}^{t_3} i_L(t)\, dt$

Energy stored in inductor during interval $t_2 \le t \le t_3$:

$$W_L = \int_{t_2}^{t_3} v_L(t)\, i_L(t)\, dt$$

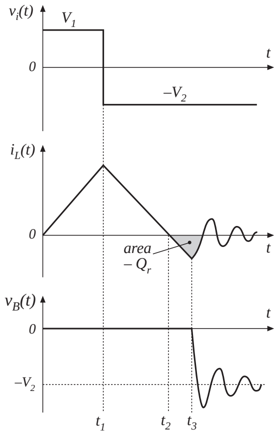
Applied inductor voltage during interval $t_2 \le t \le t_3$:

$$v_L(t) = L\,\frac{di_L(t)}{dt} = -V_2$$

Hence,

$$W_L = \int_{t_2}^{t_3} L\,\frac{di_L(t)}{dt}\, i_L(t)\, dt = \int_{t_2}^{t_3} (-V_2)\, i_L(t)\, dt$$

$$W_L = \tfrac{1}{2} L\, i_L^2(t_3) = V_2\, Q_r$$



Diode: static characteristic example

Excerpt of IXYS DSEP29-12A diode data-sheet:

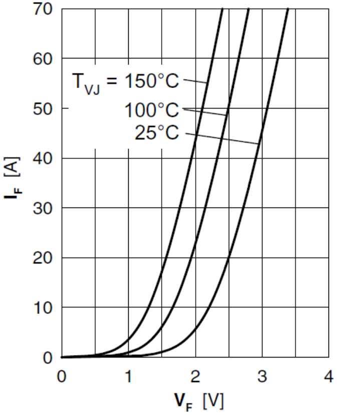


Fig. 1 Forward current I_F vs. V_F

Current sharing in parallel diodes is difficult to achieve.

Diode: recovery characteristics example

Excerpt of IXYS DSEP29-12A diode data-sheet:

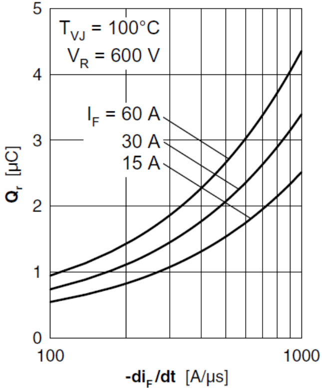


Fig. 2 Typ. reverse recovery charge Q_r versus $-di_F/dt$

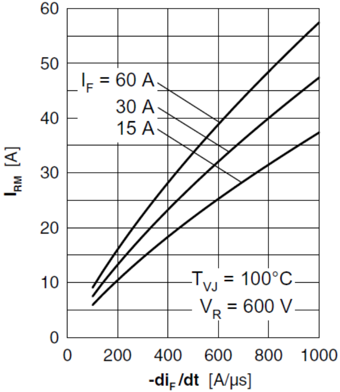


Fig. 3 Typ. peak reverse current I_{RM} versus $-di_F/dt$

Types of power diodes

Standard recovery

Reverse recovery time not specified, intended for 50/60Hz

Fast recovery and ultra-fast recovery

Reverse recovery time and recovered charge specified

Intended for converter applications

Schottky diode

A majority carrier device

Essentially no recovered charge

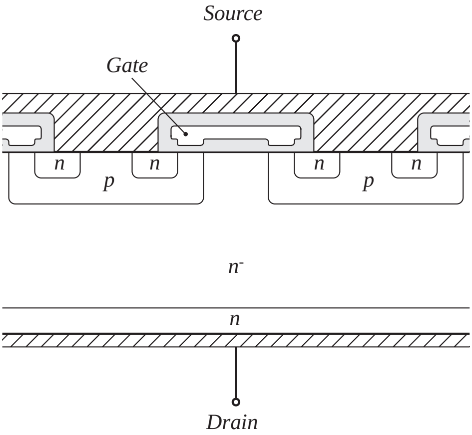
Model with equilibrium i-v characteristic, in parallel with depletion region capacitance

Restricted to low voltage (few devices can block 100V or more)

Characteristics of several commercial power rectifier diodes

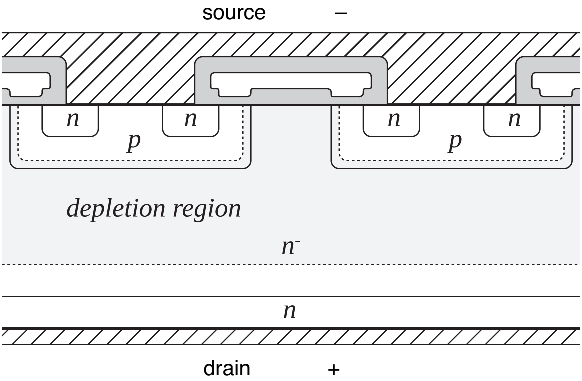
Part number	*Rated max voltage*	*Rated avg current*	*V_F (typical)*	*t_r (max)*
Fast recovery rectifiers				
1N3913	400V	30A	1.1V	400ns
SD453N25S20PC	2500V	400A	2.2V	2μs
Ultra-fast recovery rectifiers				
MUR815	150V	8A	0.975V	35ns
MUR1560	600V	15A	1.2V	60ns
RHRU100120	1200V	100A	2.6V	60ns
Schottky rectifiers				
MBR6030L	30V	60A	0.48V	
444CNQ045	45V	440A	0.69V	
30CPQ150	150V	30A	1.19V	

4.2.2. The Power MOSFET



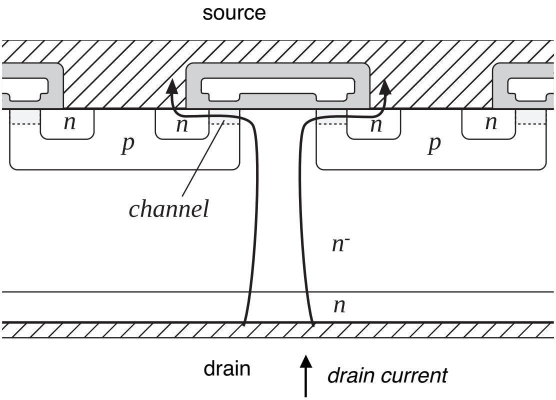
- Gate lengths approaching one micron
- Consists of many small enhancement-mode parallel-connected MOSFET cells, covering the surface of the silicon wafer
- Vertical current flow
- n-channel device is shown

MOSFET: Off state



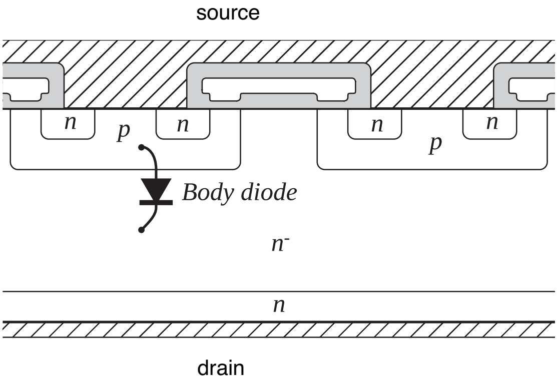
- p-n^- junction is reverse-biased
- off-state voltage appears across n^- region

MOSFET: on state



- p-n^- junction is slightly reverse-biased
- positive gate voltage induces conducting channel
- drain current flows through n^- region and conducting channel
- on resistance = total resistances of n^- region, conducting channel, source and drain contacts, etc.

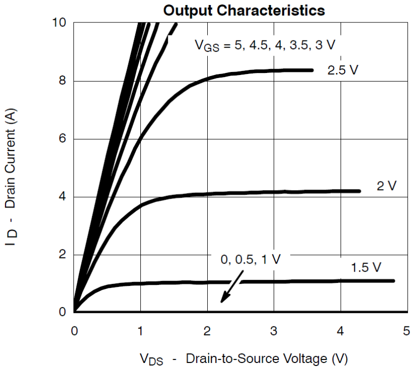
MOSFET body diode



- p-n^- junction forms an effective diode, in parallel with the channel
- negative drain-to-source voltage can forward-bias the body diode
- diode can conduct the full MOSFET rated current
- diode switching speed not optimized —body diode is slow, Q_r is large

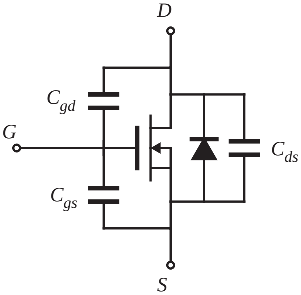
Typical MOSFET characteristics

Excerpt of Vishay Si2301DS MOSFET data-sheet:



- $V_{GS} < V_{th}$: OFF state
- $V_{GS} >> V_{th}$: ON state
- MOSFET can conduct peak current well in excess of average current rating.
- $V_{DS} <<$: D-S channel behaves like a resistor (R_{DSon}).
- $V_{DS} >>$: D-S channel behaves like a current source (linked to V_{GS} by the transconductance).

A simple MOSFET equivalent circuit

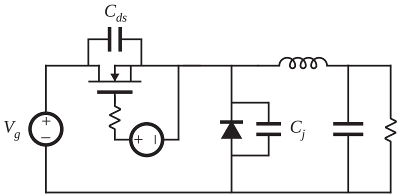


- C_{gs} : large, essentially constant
- C_{gd} : small, highly nonlinear
- C_{ds} : intermediate in value, highly nonlinear
- switching times determined by rate at which gate driver charges/discharges C_{gs} and C_{gd}

$$C_{ds}(v_{ds}) = \frac{C_0}{\sqrt{1 + \frac{v_{ds}}{V_0}}} \qquad C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0'}{\sqrt{v_{ds}}}$$

Switching loss caused by semiconductor output capacitances

Buck converter example



Energy lost during MOSFET turn-on transition
(assuming linear capacitances):

$$W_C = \frac{1}{2}\,(C_{ds} + C_j)\,V_g^2$$

MOSFET nonlinear C_{ds}

Incremental $C_{ds}(v_{ds})$ is approximated by: $C_{ds}(v_{ds}) \approx \frac{C_0'}{\sqrt{v_{ds}}}$.
The energy stored in C_{ds} at $v_{ds} = V_{DS}$:

$$W_{C_{ds}} = \int v_{ds} i_C dt = \int v_{ds} C_{ds}(v_{ds}) \frac{dv_{ds}(t)}{dt} dt = \int_0^{V_{DS}} v_{ds} C_{ds}(v_{ds}) dv_{ds}$$

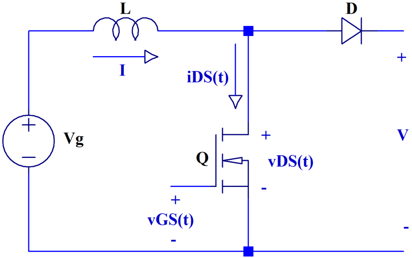
$$= \int_0^{V_{DS}} \frac{C_0'}{\sqrt{v_{ds}}} v_{ds} dv_{ds} = \int_0^{V_{DS}} C_0' \sqrt{v_{ds}} dv_{ds}$$

$$= \frac{2}{3} C_0' V_{DS}^{\frac{3}{2}} = \frac{2}{3} \frac{C_0'}{\sqrt{V_{DS}}} V_{DS}^2 = \frac{1}{2} \frac{4}{3} C_{ds}(V_{DS}) V_{Ds}^2.$$

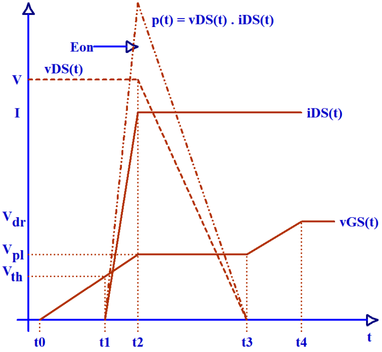
The energy loss is equivalent to the energy loss related to a voltage independant capacitor but taking $\frac{4}{3}$ of the capacitance value at V_{ds}.

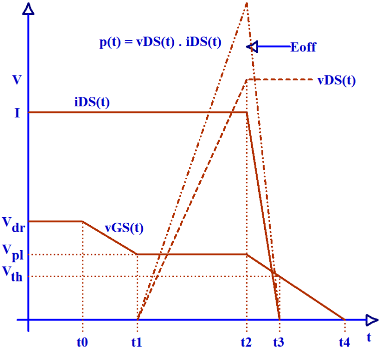
MOSFET: hard switching losses circuit example

- Boost converter considered.
- The reasoning also applied to other circuits in hard switching.
- Diode D is considered ideal in this case.



MOSFET: hard switching losses waveforms





Power losses = area E_{on} and E_{off} (energy) times f_s (switching frequency):

$P_{ON} = \frac{1}{2} V \cdot I \cdot (t_3 - t_1) \cdot f_s$ $\qquad$ $P_{OFF} = \frac{1}{2} V \cdot I \cdot (t_3 - t_1) \cdot f_s$

Rebuild the diagram.

MOSFET: hard switching losses explanations

Turn-On (left figure on previous slide):

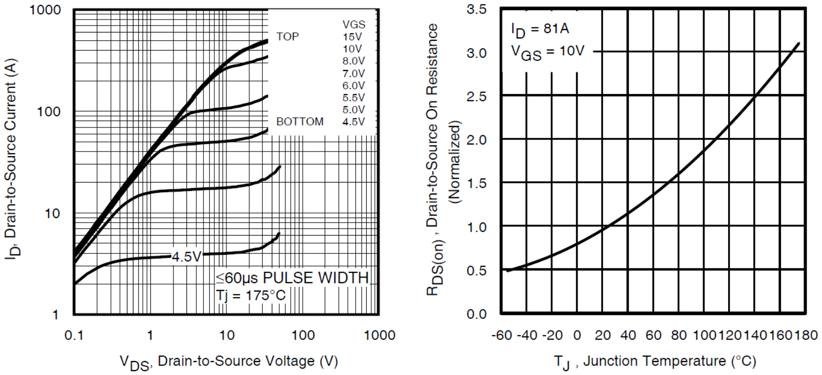
- $t_0 \rightarrow t_1$: the gate voltage $v_{GS}(t)$ rises from 0 to V_{th}.
- $t_1 \rightarrow t_2$: the drain current $i_{DS}(t)$ rises according to $v_{GS}(t)$ change (linked by the transconductance). Once $i_{DS}(t)$ reaches I, the transistor carries the full load current.
- $t_2 \rightarrow t_3$: $v_{GS}(t)$ stays at the "plateau" voltage V_{pl} due to the Miller effect and the drain voltage $v_{DS}(t)$ falls linearly.
- $t_3 \rightarrow t_4$: once $v_{DS}(t)$ reaches $0V$ at t_3, $v_{GS}(t)$ continues to rise up to V_{dr}.

Turn-Off (right figure on previous slide):

- $t_0 \rightarrow t_1$: $v_{GS}(t)$ falls from V_{dr} to V_{pl}.
- $t_1 \rightarrow t_2$: when $v_{GS}(t)$ reaches V_{pl}, $v_{DS}(t)$ starts rising linearly. $v_{GS}(t)$ stays at V_{pl} due to the Miller effect.
- $t_2 \rightarrow t_3$: once $v_{DS}(t)$ reaches V, $v_{GS}(t)$ starts falling again and $i_{DS}(t)$ also starts falling accordingly (linked by the transconductance).
- $t_3 \rightarrow t_4$: once $v_{GS}(t)$ reaches V_{th}, $i_{DS}(t)$ reaches $0V$ and $v_{GS}(t)$ goes to $0V$.

MOSFET: static characteristics example

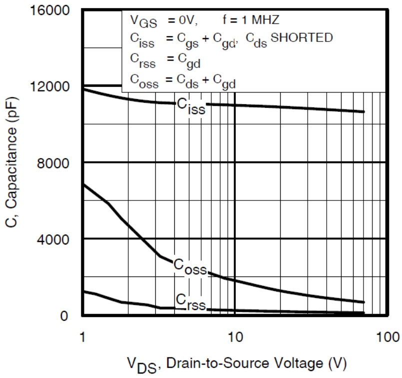
Excerpt of IR IRFP4668PbF MOSFET data-sheet:

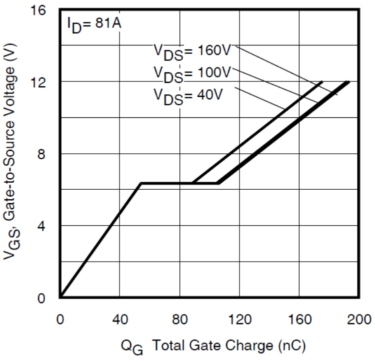


R_{DSon} has positive temperature coefficient, MOSFETs are therefore easy to parallel.

MOSFET: dynamic characteristics example

Excerpt of IR IRFP4668PbF MOSFET data-sheet:





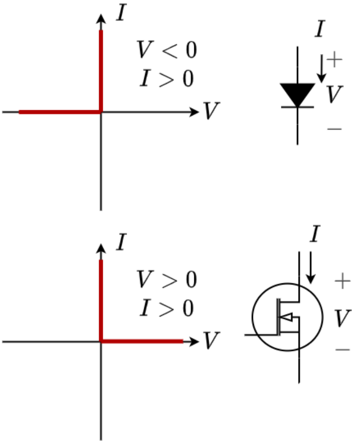
Characteristics of several commercial power MOSFETs

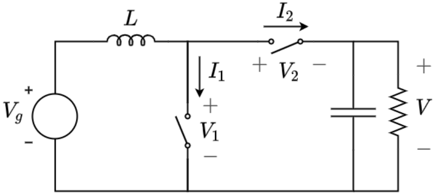
Part number	*Rated max voltage*	*Rated avg current*	R_{on}	Q_g *(typical)*
IRFZ48	60V	50A	0.018Ω	110nC
IRF510	100V	5.6A	0.54Ω	8.3nC
IRF540	100V	28A	0.077Ω	72nC
APT10M25BNR	100V	75A	0.025Ω	171nC
IRF740	400V	10A	0.55Ω	63nC
MTM15N40E	400V	15A	0.3Ω	110nC
APT5025BN	500V	23A	0.25Ω	83nC
APT1001RBNR	1000V	11A	1.0Ω	150nC

MOSFET: conclusions

- A majority-carrier device: fast switching speed
- Typical switching frequencies: tens and hundreds of kHz
- On-resistance increases rapidly with rated blocking voltage
- Easy to drive
- The device of choice for blocking voltages less than 500V
- 1000V devices are available, but are useful only at low power levels (100W)
- Part number is selected on the basis of on-resistance rather than current rating

Switch selection: controlled switch or diode?

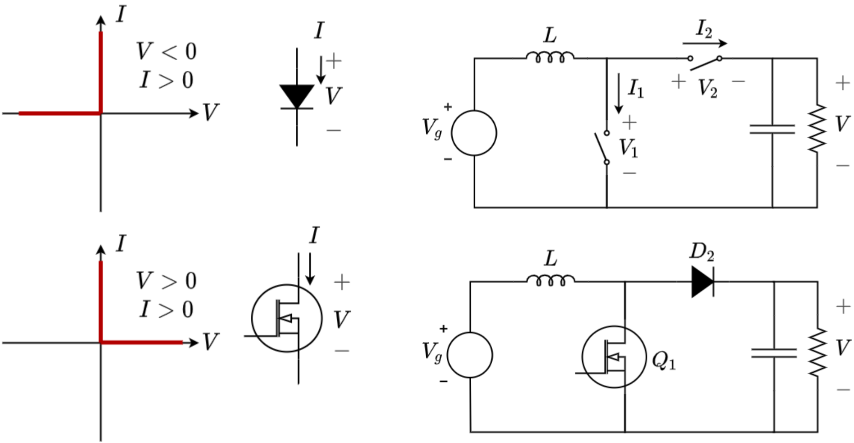




- If $V > 0$ and $I > 0 \Rightarrow$ a controlled switch is required.
- If $V < 0$ and $I > 0 \Rightarrow$ a diode can be used.

Another example: CUK converter

Switch selection: controlled switch or diode?



- If $V > 0$ and $I > 0 \Rightarrow$ a controlled switch is required.
- If $V < 0$ and $I > 0 \Rightarrow$ a diode can be used.

Another example: CUK converter

Other power semi-conductors (brief overview)

Thyristor: high voltage, high current, switches off at zero current,

GTO (gate turn off Thyristor): similar to Thyristor but can be switched off with the gate signal,

IGBT (Isolated Gate Bipolar Transistor): high voltage, high current, controlled like a MOSFET,

BJT transistor: not often used, replaced by MOSFET,

Schottky diode: diode with higher conduction and switching performances but lower breakdown voltage,

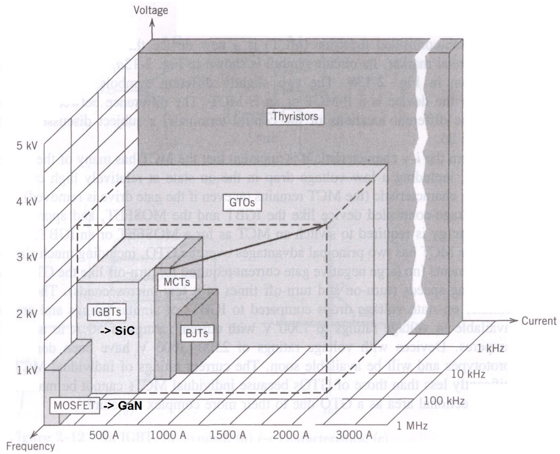
SiC diode: emerging component that could/will replace diodes,

SiC transistor: emerging component that could/will replace IGBT,

GaN transistor: emerging component that could/will replace MOSFET.

Other power semi-conductors

Excerpt of [4]:



Chapter 5: The Discontinuous Conduction Mode

Introduction to Discontinuous Conduction Mode (DCM)

- Occurs because switching ripple in inductor current or capacitor voltage causes polarity of applied switch current or voltage to reverse, such that the current- or voltage-unidirectional assumptions made in realizing the switch are violated.
- Commonly occurs in dc-dc converters and rectifiers, having single-quadrant switches. May also occur in converters having two-quadrant switches.
- Typical example: dc-dc converter operating at light load (small load current). Sometimes, dc-dc converters and rectifiers are purposely designed to operate in DCM at all loads.
- Properties of converters change radically when DCM is entered:

  M becomes load-dependent

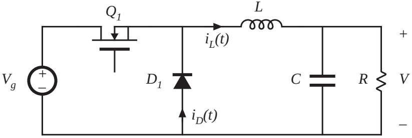
  Output impedance is increased

  Dynamics are altered

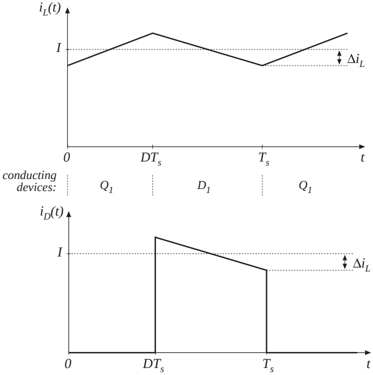
  Control of output voltage may be lost when load is removed

5.1. Origin of the discontinuous conduction mode, and mode boundary

Buck converter example, with single-quadrant switches



continuous conduction mode (CCM)



Minimum diode current is $(I - \Delta i_L)$

Dc component $I = V/R$

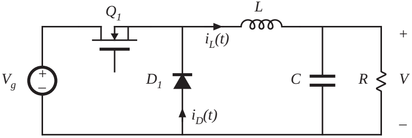
Current ripple is

$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

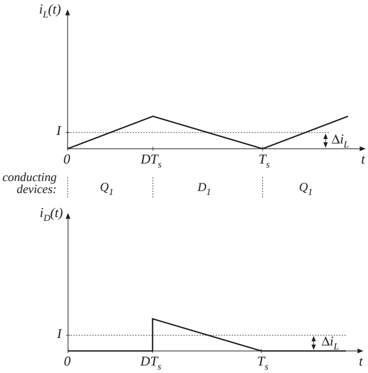
Note that I depends on load, but Δi_L does not.

Reduction of load current

Increase R, until $I = \Delta i_L$



CCM-DCM boundary



Minimum diode current is $(I - \Delta i_L)$

Dc component $I = V/R$

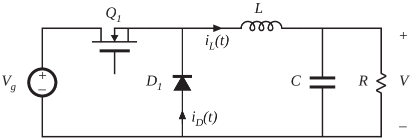
Current ripple is

$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

Note that I depends on load, but Δi_L does not.

Further reduce load current

Increase R some more, such that $I < \Delta i_L$

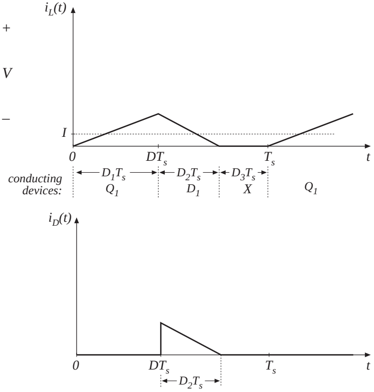


Minimum diode current is $(I - \Delta i_L)$
Dc component $I = V/R$
Current ripple is

$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g\, DD'T_s}{2L}$$

Note that I depends on load, but Δi_L does not.
The load current continues to be positive and non-zero.

Discontinuous conduction mode



Mode boundary

$$I > \Delta i_L \quad for\ CCM$$
$$I < \Delta i_L \quad for\ DCM$$

Insert buck converter expressions for I and Δi_L :

$$\frac{DV_g}{R} < \frac{DD'T_sV_g}{2L}$$

Simplify:

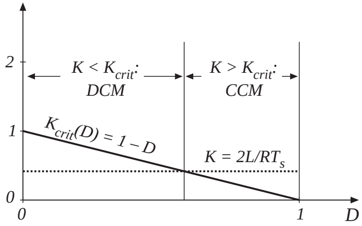
$$\frac{2L}{RT_s} < D'$$

This expression is of the form

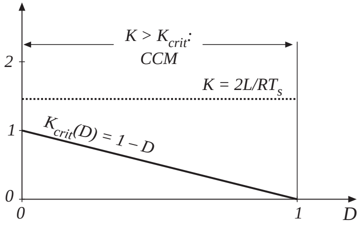
$$K < K_{crit}(D) \qquad for\ DCM$$
$$\text{where} \quad K = \frac{2L}{RT_s} \quad and \quad K_{crit}(D) = D'$$

K and K_{crit} vs. D

for $K < 1$:



for $K > 1$:



Critical load resistance R_{crit}

Solve K_{crit} equation for load resistance R:

$$R < R_{crit}(D) \qquad \textit{for CCM}$$
$$R > R_{crit}(D) \qquad \textit{for DCM}$$

where $$R_{crit}(D) = \frac{2L}{D'T_s}$$

Summary: mode boundary

$$K > K_{crit}(D) \quad \text{or} \quad R < R_{crit}(D) \quad \text{for CCM}$$
$$K < K_{crit}(D) \quad \text{or} \quad R > R_{crit}(D) \quad \text{for DCM}$$

Table 5.1. CCM-DCM mode boundaries for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	$\max_{0 \le D \le 1}(K_{crit})$	$R_{crit}(D)$	$\min_{0 \le D \le 1}(R_{crit})$
Buck	$(1 - D)$	1	$\frac{2L}{(1-D)T_s}$	$2\frac{L}{T_s}$
Boost	$D(1 - D)^2$	$\frac{4}{27}$	$\frac{2L}{D(1-D)^2 T_s}$	$\frac{27}{2}\frac{L}{T_s}$
Buck-boost	$(1 - D)^2$	1	$\frac{2L}{(1-D)^2 T_s}$	$2\frac{L}{T_s}$

5.2. Analysis of the conversion ratio *M(D,K)*

Analysis techniques for the discontinuous conduction mode:

Inductor volt-second balance

$$\langle v_L \rangle = \frac{1}{T_s} \int_0^{T_s} v_L(t)\, dt = 0$$

Capacitor charge balance

$$\langle i_C \rangle = \frac{1}{T_s} \int_0^{T_s} i_C(t)\, dt = 0$$

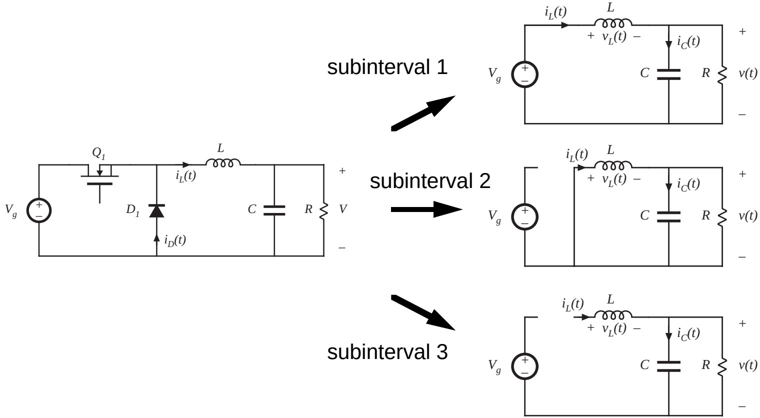
Small ripple approximation sometimes applies:

$$v(t) \approx V \quad \text{because} \quad \Delta v \ll V$$

$$i(t) \approx I \ \text{ is a poor approximation when } \ \Delta i > I$$

Converter steady-state equations obtained via charge balance on each capacitor and volt-second balance on each inductor. Use care in applying small ripple approximation.

Example: Analysis of DCM buck converter $M(D,K)$

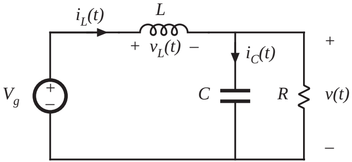


Subinterval 1

$$v_L(t) = V_g - v(t)$$
$$i_C(t) = i_L(t) - v(t) / R$$

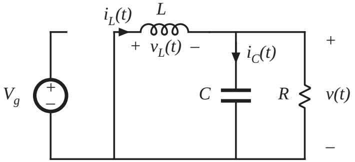
Small ripple approximation for *v(t)* (but not for *i(t)*!):

$$v_L(t) \approx V_g - V$$
$$i_C(t) \approx i_L(t) - V / R$$



Subinterval 2

$$v_L(t) = -\,v(t)$$
$$i_C(t) = i_L(t) - v(t)\;/\;R$$



Small ripple approximation for $v(t)$ but not for $i(t)$:

$$v_L(t) \approx -\,V$$
$$i_C(t) \approx i_L(t) - V\;/\;R$$

Subinterval 3

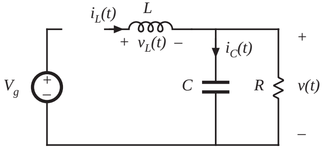
$v_L = 0, \quad i_L = 0$

$i_C(t) = i_L(t) - v(t) / R$

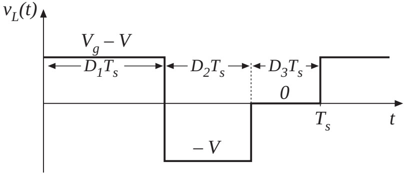
Small ripple approximation:

$v_L(t) = 0$

$i_C(t) = -V / R$



Inductor volt-second balance



Volt-second balance:

$$\langle v_L(t) \rangle = D_1(V_g - V) + D_2(-V) + D_3(0) = 0$$

Solve for V:

$$V = V_g \frac{D_1}{D_1 + D_2}$$

note that D_2 is unknown

Capacitor charge balance

node equation:

$$i_L(t) = i_C(t) + V / R$$

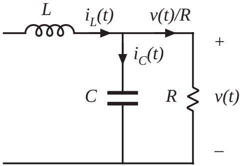
capacitor charge balance:

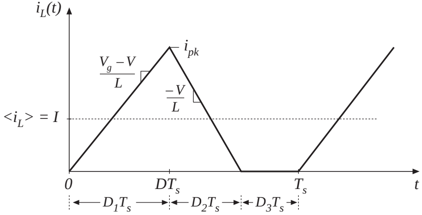
$$\langle i_C \rangle = 0$$

hence

$$\langle i_L \rangle = V / R$$

must compute dc component of inductor current and equate to load current (for this buck converter example)





Inductor current waveform

peak current:

$$i_L(D_1T_s) = i_{pk} = \frac{V_g - V}{L} D_1T_s$$

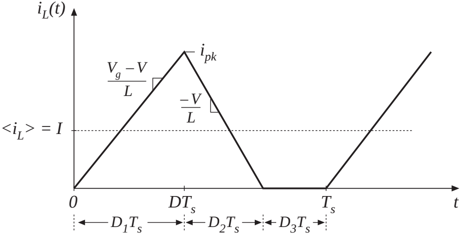
average current:

$$\langle i_L \rangle = \frac{1}{T_s} \int_0^{T_s} i_L(t)\, dt$$

triangle area formula:

$$\int_0^{T_s} i_L(t)\, dt = \frac{1}{2}\, i_{pk}\, (D_1 + D_2)T_s$$

$$\langle i_L \rangle = (V_g - V)\, \frac{D_1T_s}{2L}\, (D_1 + D_2)$$



equate dc component to dc load current:

$$\frac{V}{R} = \frac{D_1T_s}{2L}\, (D_1 + D_2)\, (V_g - V)$$

Solution for V

Two equations and two unknowns (V and D_2):

$$V = V_g \frac{D_1}{D_1 + D_2}$$ (from inductor volt-second balance)

$$\frac{V}{R} = \frac{D_1 T_s}{2L}(D_1 + D_2)(V_g - V)$$ (from capacitor charge balance)

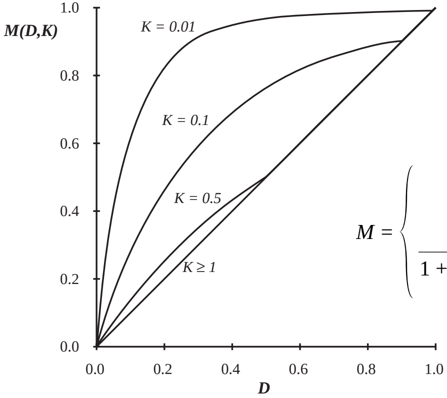
Eliminate D_2 , solve for V :

$$\frac{V}{V_g} = \frac{2}{1 + \sqrt{1 + 4K / D_1^2}}$$

where $K = 2L / RT_s$

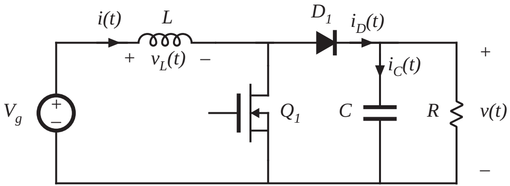
valid for $K < K_{crit}$

Buck converter *M(D,K)*



$$M = \begin{cases} D & \text{for } K > K_{crit} \\ \dfrac{2}{1+\sqrt{1+4K/D^2}} & \text{for } K < K_{crit} \end{cases}$$

5.3. Boost converter example



Mode boundary:

$$I > \Delta i_L \quad \textit{for CCM}$$
$$I < \Delta i_L \quad \textit{for DCM}$$

Previous CCM soln:

$$I = \frac{V_g}{D'^2 R} \qquad \Delta i_L = \frac{V_g}{2L} D T_s$$

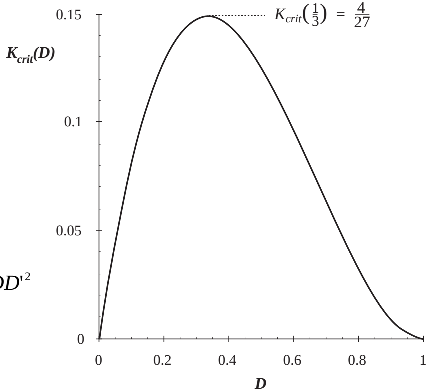
Mode boundary

$$\frac{V_g}{D'^2 R} > \frac{D T_s V_g}{2L} \qquad \text{for CCM}$$

$$\frac{2L}{R T_s} > D D'^2 \qquad \text{for CCM}$$

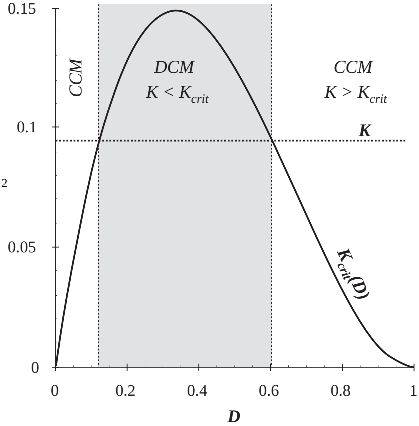
$$K > K_{crit}(D) \qquad \text{for CCM}$$
$$K < K_{crit}(D) \qquad \text{for DCM}$$

where $K = \dfrac{2L}{R T_s}$ and $K_{crit}(D) = D D'^2$

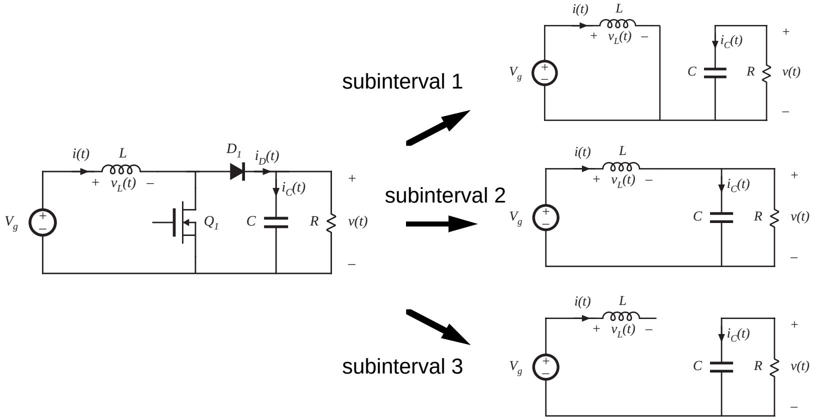


Mode boundary

$$K > K_{crit}(D) \qquad \text{for CCM}$$
$$K < K_{crit}(D) \qquad \text{for DCM}$$
$$\text{where} \quad K = \frac{2L}{RT_s} \quad \text{and} \quad K_{crit}(D) = DD'^2$$



Conversion ratio: DCM boost

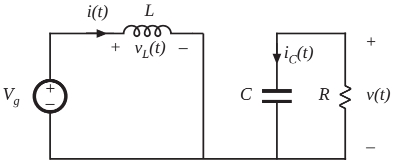


Subinterval 1

$$v_L(t) = V_g$$
$$i_C(t) = -\,v(t)\,/\,R$$

Small ripple approximation for *v(t)* (but not for *i(t)*!):

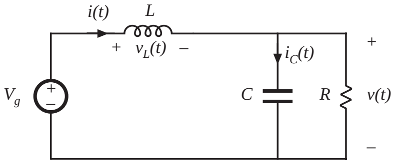
$$v_L(t) \approx V_g$$
$$i_C(t) \approx -\,V\,/\,R$$



$0 < t < D_1T_s$

Subinterval 2

$$v_L(t) = V_g - v(t)$$
$$i_C(t) = i(t) - v(t) / R$$



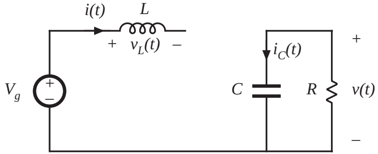
Small ripple approximation for $v(t)$ but not for $i(t)$:

$$v_L(t) \approx V_g - V$$
$$i_C(t) \approx i(t) - V / R$$

$$D_1 T_s < t < (D_1 + D_2) T_s$$

Subinterval 3

$v_L = 0, \quad i = 0$
$i_C(t) = -\,v(t) \,/\, R$

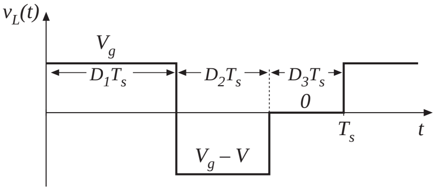


Small ripple approximation:

$v_L(t) = 0$
$i_C(t) = -\,V \,/\, R$

$(D_1 + D_2)T_s \;<\; t \;<\; T_s$

Inductor volt-second balance



Volt-second balance:

$$D_1V_g + D_2(V_g - V) + D_3(0) = 0$$

Solve for V:

$$V = \frac{D_1 + D_2}{D_2} V_g$$

note that D_2 is unknown

Capacitor charge balance

node equation:

$$i_D(t) = i_C(t) + v(t) / R$$

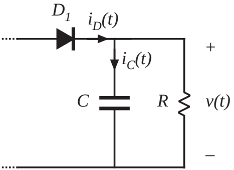
capacitor charge balance:

$$\langle i_C \rangle = 0$$

hence

$$\langle i_D \rangle = V / R$$

must compute dc component of diode current and equate to load current (for this boost converter example)



Inductor and diode current waveforms

peak current:

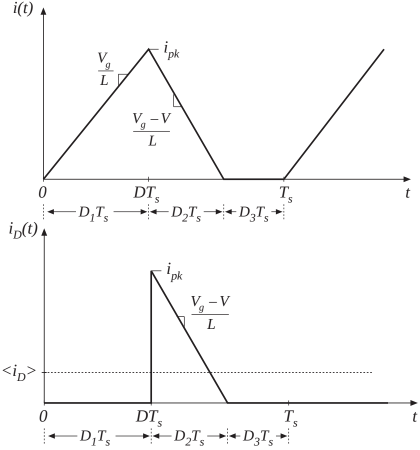
$$i_{pk} = \frac{V_g}{L} D_1 T_s$$

average diode current:

$$\left\langle i_D \right\rangle = \frac{1}{T_s} \int_0^{T_s} i_D(t)\, dt$$

triangle area formula:

$$\int_0^{T_s} i_D(t)\, dt = \frac{1}{2}\, i_{pk}\, D_2 T_s$$



Equate diode current to load current

average diode current:

$$\left\langle i_D \right\rangle = \frac{1}{T_s}\left(\frac{1}{2}\, i_{pk}\, D_2 T_s\right) = \frac{V_g D_1 D_2 T_s}{2L}$$

equate to dc load current:

$$\frac{V_g D_1 D_2 T_s}{2L} = \frac{V}{R}$$

Solution for V

Two equations and two unknowns (V and D_2):

$$V = \frac{D_1 + D_2}{D_2} V_g \qquad \text{(from inductor volt-second balance)}$$

$$\frac{V_g D_1 D_2 T_s}{2L} = \frac{V}{R} \qquad \text{(from capacitor charge balance)}$$

Eliminate D_2 , solve for V. From volt-sec balance eqn:

$$D_2 = D_1 \frac{V_g}{V - V_g}$$

Substitute into charge balance eqn, rearrange terms:

$$V^2 - VV_g - \frac{V_g^2 D_1^2}{K} = 0$$

Solution for V

$$V^2 - VV_g - \frac{V_g^2 D_1^2}{K} = 0$$

Use quadratic formula:

$$\frac{V}{V_g} = \frac{1 \pm \sqrt{1 + 4D_1^2 / K}}{2}$$

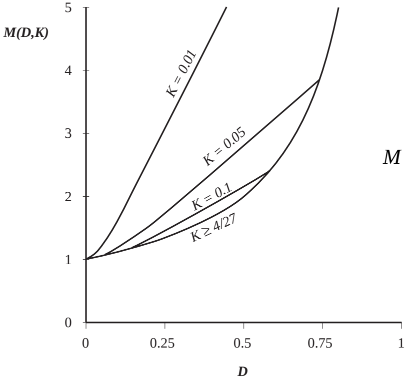
Note that one root leads to positive V, while other leads to negative V. Select positive root:

$$\frac{V}{V_g} = M(D_1,K) = \frac{1 + \sqrt{1 + 4D_1^2 / K}}{2}$$

where $K = 2L / RT_s$
valid for $K < K_{crit}(D)$

Transistor duty cycle D = interval *1* duty cycle D_1

Boost converter characteristics



$$M = \begin{cases} \dfrac{1}{1-D} & \text{for } K > K_{crit} \\ \dfrac{1+\sqrt{1+4D^2/K}}{2} & \text{for } K < K_{crit} \end{cases}$$

Approximate M in DCM:

$$M \approx \frac{1}{2} + \frac{D}{\sqrt{K}}$$

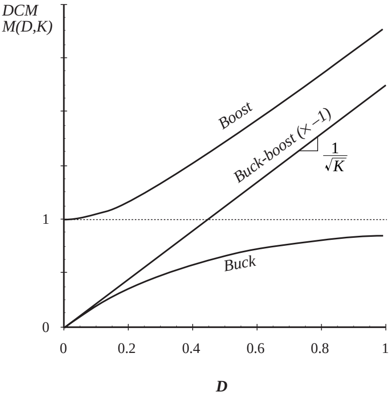
Summary of DCM characteristics

Table 5.2. Summary of CCM-DCM characteristics for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	DCM $M(D,K)$	DCM $D_2(D,K)$	CCM $M(D)$
Buck	$(1-D)$	$\frac{2}{1+\sqrt{1+4K/D^2}}$	$\frac{K}{D}M(D,K)$	D
Boost	$D(1-D)^2$	$\frac{1+\sqrt{1+4D^2/K}}{2}$	$\frac{K}{D}M(D,K)$	$\frac{1}{1-D}$
Buck-boost	$(1-D)^2$	$-\frac{D}{\sqrt{K}}$	$\sqrt{K}$	$-\frac{D}{1-D}$

with $K = 2L / RT_s$. *DCM occurs for* $K < K_{crit}$.

Summary of DCM characteristics



- DCM buck and boost characteristics are asymptotic to M = 1 and to the DCM buck-boost characteristic
- DCM buck-boost characteristic is linear
- CCM and DCM characteristics intersect at mode boundary. Actual M follows characteristic having larger magnitude
- DCM boost characteristic is nearly linear

Summary of key points

1. The discontinuous conduction mode occurs in converters containing current- or voltage-unidirectional switches, when the inductor current or capacitor voltage ripple is large enough to cause the switch current or voltage to reverse polarity.
2. Conditions for operation in the discontinuous conduction mode can be found by determining when the inductor current or capacitor voltage ripples and dc components cause the switch on-state current or off-state voltage to reverse polarity.
3. The dc conversion ratio M of converters operating in the discontinuous conduction mode can be found by application of the principles of inductor volt-second and capacitor charge balance.

Summary of key points

4. Extra care is required when applying the small-ripple approximation. Some waveforms, such as the output voltage, should have small ripple which can be neglected. Other waveforms, such as one or more inductor currents, may have large ripple that cannot be ignored.
5. The characteristics of a converter changes significantly when the converter enters DCM. The output voltage becomes load-dependent, resulting in an increase in the converter output impedance.

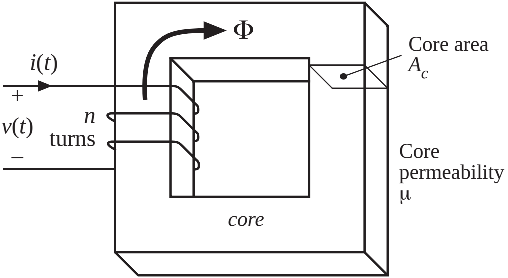
Chapter 13: Basic Magnetics Theory

Example: a simple inductor

Faraday's law:

For each turn of wire, we can write

$$v_{turn}(t) = \frac{d\Phi(t)}{dt}$$



Total winding voltage is

$$v(t) = nv_{turn}(t) = n\,\frac{d\Phi(t)}{dt}$$

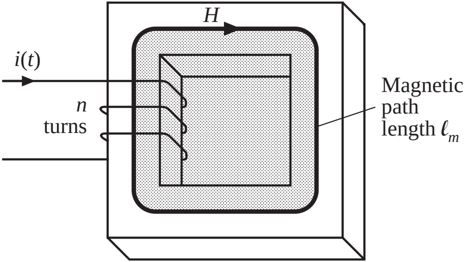
Express in terms of the average flux density $B(t) = \mathscr{F}(t)/A_c$

$$v(t) = nA_c\,\frac{dB(t)}{dt}$$

Inductor example: Ampere's law

Choose a closed path which follows the average magnetic field line around the interior of the core. Length of this path is called the *mean magnetic path length* ℓ_m.

For uniform field strength $H(t)$, the core MMF around the path is $H\,\ell_m$.



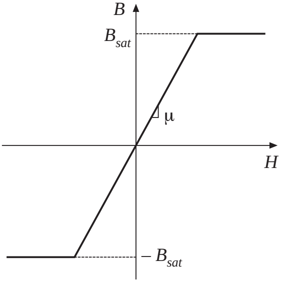
Winding contains n turns of wire, each carrying current $i(t)$. The net current passing through the path interior (i.e., through the core window) is $ni(t)$.

From Ampere's law, we have

$$H(t)\,\ell_m = n\,i(t)$$

Inductor example: core material model

$$B = \begin{cases} B_{sat} & \text{for } H \geq B_{sat}/\mu \\ \mu H & \text{for } |H| < B_{sat}/\mu \\ -B_{sat} & \text{for } H \leq -B_{sat}/\mu \end{cases}$$



Find winding current at onset of saturation: substitute $i = I_{sat}$ and $H = B_{sat}/\mu$ into equation previously derived via Ampere's law. Result is

$$I_{sat} = \frac{B_{sat}\ell_m}{\mu n}$$

Electrical terminal characteristics

We have:

$$v(t) = nA_c \frac{dB(t)}{dt} \qquad H(t)\,\ell_m = n\,i(t) \qquad B = \begin{cases} B_{sat} & \text{for } H \ge B_{sat}/\mu \\ \mu H & \text{for } |H| < B_{sat}/\mu \\ -B_{sat} & \text{for } H \le -B_{sat}/\mu \end{cases}$$

Eliminate B and H, and solve for relation between v and i. For $|\,i\,| < I_{sat}$,

$$v(t) = \mu n A_c \frac{dH(t)}{dt} \longrightarrow v(t) = \frac{\mu n^2 A_c}{\ell_m} \frac{di(t)}{dt}$$

which is of the form

$$v(t) = L\,\frac{di(t)}{dt} \qquad \text{with} \qquad L = \frac{\mu n^2 A_c}{\ell_m}$$

—an inductor

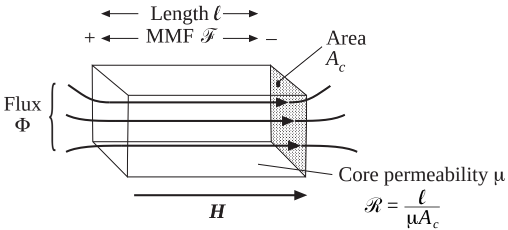
For $|\,i\,| > I_{sat}$ the flux density is constant and equal to B_{sat}. Faraday's law then predicts

$$v(t) = nA_c \frac{dB_{sat}}{dt} = 0$$

—saturation leads to short circuit

13.1.2 Magnetic circuits

Uniform flux and magnetic field inside a rectangular element:



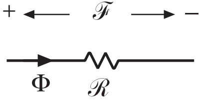
MMF between ends of element is

$$\mathscr{F} = H\ell$$

Since $H = B / \mu$ and $B = \Phi / A_c$, we can express $\mathscr{F}$ as

$$\mathscr{F} = \Phi\mathscr{R} \qquad \text{with} \qquad \mathscr{R} = \frac{\ell}{\mu A_c}$$

A corresponding model:



$\mathscr{R}$ = reluctance of element

Magnetic circuits: magnetic structures composed of multiple windings and heterogeneous elements

- Represent each element with reluctance
- Windings are sources of MMF
- MMF → voltage, flux → current
- Solve magnetic circuit using Kirchoff's laws, etc.

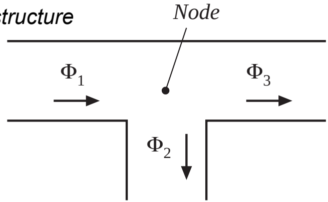
Magnetic analog of Kirchoff's current law

Divergence of $\boldsymbol{B} = 0$

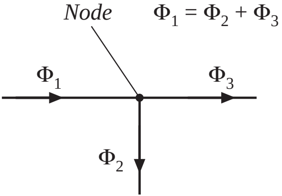
Flux lines are continuous and cannot end

Total flux entering a node must be zero

Physical structure



Magnetic circuit



Magnetic analog of Kirchoff's voltage law

Follows from Ampere's law:

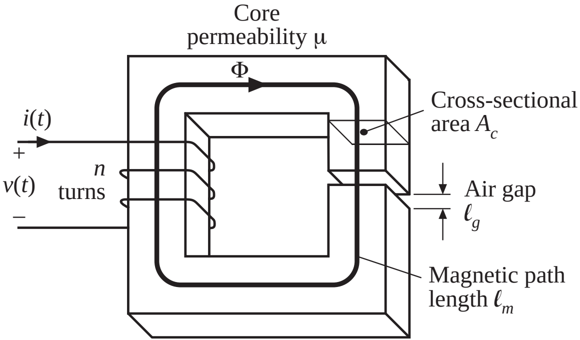
$$\oint_{closed\ path} \boldsymbol{H} \cdot d\boldsymbol{\ell} = \text{total current passing through interior of path}$$

Left-hand side: sum of MMF's across the reluctances around the closed path

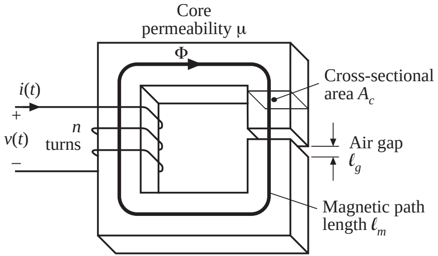
Right-hand side: currents in windings are sources of MMF's. An n-turn winding carrying current $i(t)$ is modeled as an MMF (voltage) source, of value $ni(t)$.

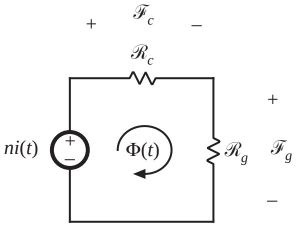
Total MMF's around the closed path add up to zero.

Example: inductor with air gap



Magnetic circuit model





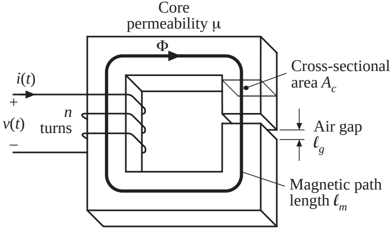
$$\mathscr{F}_c + \mathscr{F}_g = ni$$

$$ni = \Phi\left(\mathscr{R}_c + \mathscr{R}_g\right)$$

$$\mathscr{R}_c = \frac{\ell_c}{\mu A_c}$$

$$\mathscr{R}_g = \frac{\ell_g}{\mu_0 A_c}$$

Solution of model

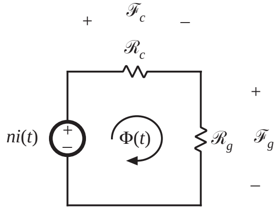


Faraday's law: $$v(t) = n\,\frac{d\Phi(t)}{dt}$$

Substitute for Φ: $$v(t) = \frac{n^2}{\mathcal{R}_c + \mathcal{R}_g}\,\frac{di(t)}{dt}$$

Hence inductance is

$$L = \frac{n^2}{\mathcal{R}_c + \mathcal{R}_g}$$



$$ni = \Phi\left(\mathcal{R}_c + \mathcal{R}_g\right)$$

$$\mathcal{R}_c = \frac{\ell_c}{\mu A_c}$$

$$\mathcal{R}_g = \frac{\ell_g}{\mu_0 A_c}$$

Effect of air gap

$$ni = \Phi\left(\mathcal{R}_c + \mathcal{R}_g\right)$$

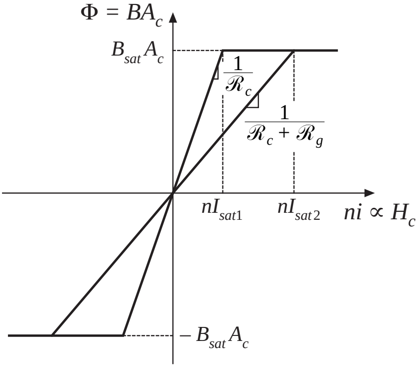
$$L = \frac{n^2}{\mathcal{R}_c + \mathcal{R}_g}$$

$$\Phi_{sat} = B_{sat} A_c$$

$$I_{sat} = \frac{B_{sat} A_c}{n}\left(\mathcal{R}_c + \mathcal{R}_g\right)$$

Effect of air gap:

- decrease inductance
- increase saturation current
- inductance is less dependent on core permeability



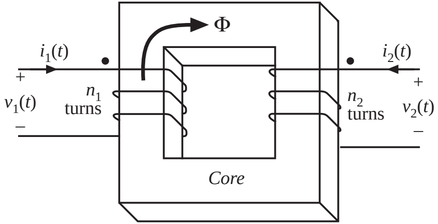
13.2 Transformer modeling

Two windings, no air gap:

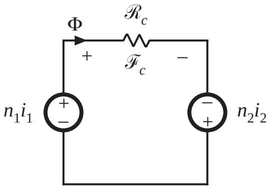
$$\mathscr{R} = \frac{\ell_m}{\mu A_c}$$

$$\mathscr{F}_c = n_1 i_1 + n_2 i_2$$

$$\Phi \mathscr{R} = n_1 i_1 + n_2 i_2$$



Magnetic circuit model:



13.2.1 The ideal transformer

In the ideal transformer, the core reluctance $\mathscr{R}$ approaches zero.

MMF $\mathscr{F}_c = \Phi\,\mathscr{R}$ also approaches zero. We then obtain

$$0 = n_1 i_1 + n_2 i_2$$

Also, by Faraday's law,

$$v_1 = n_1 \frac{d\Phi}{dt}$$

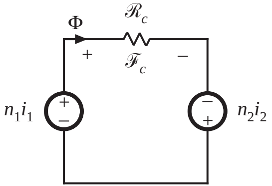
$$v_2 = n_2 \frac{d\Phi}{dt}$$

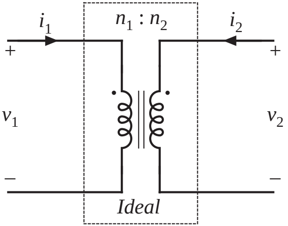
Eliminate Φ :

$$\frac{d\Phi}{dt} = \frac{v_1}{n_1} = \frac{v_2}{n_2}$$

Ideal transformer equations:

$$\frac{v_1}{n_1} = \frac{v_2}{n_2} \quad \text{and} \quad n_1 i_1 + n_2 i_2 = 0$$

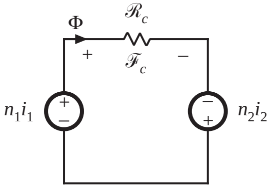




13.2.2 The magnetizing inductance

For nonzero core reluctance, we obtain

$$\Phi \mathcal{R} = n_1 i_1 + n_2 i_2 \quad \text{with} \quad v_1 = n_1 \frac{d\Phi}{dt}$$



Eliminate Φ:

$$v_1 = \frac{n_1^2}{\mathcal{R}} \frac{d}{dt}\left[i_1 + \frac{n_2}{n_1} i_2 \right]$$

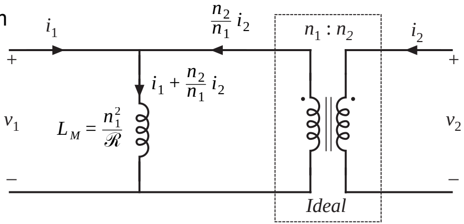
This equation is of the form

$$v_1 = L_M \frac{di_M}{dt}$$

with

$$L_M = \frac{n_1^2}{\mathcal{R}}$$

$$i_M = i_1 + \frac{n_2}{n_1} i_2$$



Magnetizing inductance: discussion

- Models magnetization of core material
- A real, physical inductor, that exhibits saturation and hysteresis
- If the secondary winding is disconnected:

  we are left with the primary winding on the core

  primary winding then behaves as an inductor

  the resulting inductor is the magnetizing inductance, referred to the primary winding
- Magnetizing current causes the ratio of winding currents to differ from the turns ratio

Transformer saturation

- Saturation occurs when core flux density $B(t)$ exceeds saturation flux density B_{sat}.
- When core saturates, the magnetizing current becomes large, the impedance of the magnetizing inductance becomes small, and the windings are effectively shorted out.
- Large winding currents $i_1(t)$ and $i_2(t)$ ***do not*** necessarily lead to saturation. If

$$0 = n_1 i_1 + n_2 i_2$$

  then the magnetizing current is zero, and there is no net magnetization of the core.
- Saturation is caused by excessive applied volt-seconds

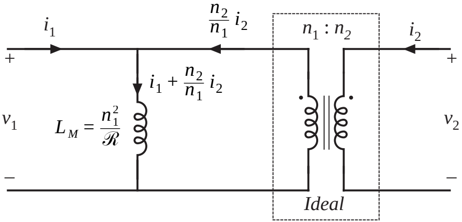
Saturation vs. applied volt-seconds

Magnetizing current depends on the integral of the applied winding voltage:

$$i_M(t) = \frac{1}{L_M} \int v_1(t)\,dt$$

Flux density is proportional:

$$B(t) = \frac{1}{n_1 A_c} \int v_1(t)\,dt$$

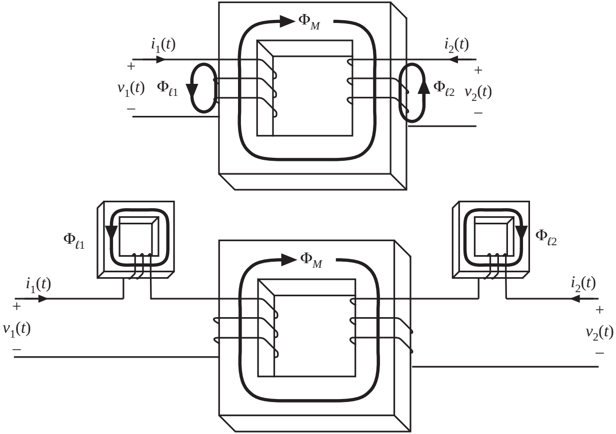


Flux density becomes large, and core saturates, when the applied volt-seconds λ_1 are too large, where

$$\lambda_1 = \int_{t_1}^{t_2} v_1(t)\,dt$$

limits of integration chosen to coincide with positive portion of applied voltage waveform

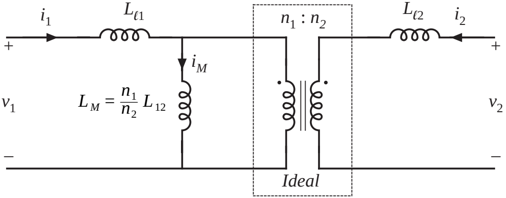
13.2.3 Leakage inductances



Transformer model, including leakage inductance

Terminal equations can be written in the form

$$\begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1(t) \\ i_2(t) \end{bmatrix}$$



mutual inductance:

$$L_{12} = \frac{n_1 n_2}{\mathscr{R}} = \frac{n_2}{n_1} L_M$$

primary and secondary self-inductances:

$$L_{11} = L_{\ell 1} + \frac{n_1}{n_2} L_{12}$$

$$L_{22} = L_{\ell 2} + \frac{n_2}{n_1} L_{12}$$

effective turns ratio $\quad n_e = \sqrt{\frac{L_{22}}{L_{11}}}$

coupling coefficient $\quad k = \frac{L_{12}}{\sqrt{L_{11} L_{22}}}$

13.3 Loss mechanisms in magnetic devices

Low-frequency losses:

- Dc copper loss
- Core loss: hysteresis loss

High-frequency losses: the skin effect

- Core loss: classical eddy current losses
- Eddy current losses in ferrite cores

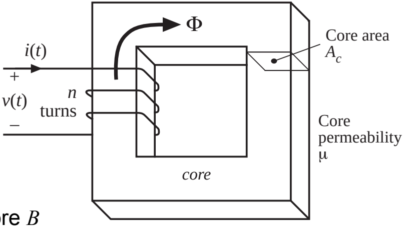
High frequency copper loss: the proximity effect

- Proximity effect: high frequency limit
- MMF diagrams, losses in a layer, and losses in basic multilayer windings
- Effect of PWM waveform harmonics

13.3.1 Core loss

Energy per cycle W flowing into n-turn winding of an inductor, excited by periodic waveforms of frequency f:

$$W = \int_{one\ cycle} v(t)i(t)\,dt$$



Relate winding voltage and current to core B and H via Faraday's law and Ampere's law:

$$v(t) = nA_c \frac{dB(t)}{dt} \qquad H(t)\ell_m = ni(t)$$

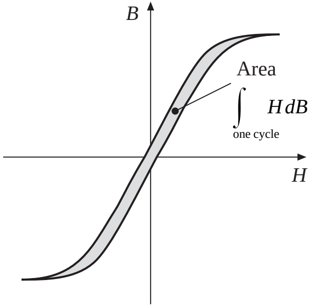
Substitute into integral:

$$W = \int_{one\ cycle} \left(nA_c \frac{dB(t)}{dt}\right)\left(\frac{H(t)\ell_m}{n}\right)dt$$

$$= \left(A_c \ell_m\right) \int_{one\ cycle} H\,dB$$

Core loss: Hysteresis loss

$$W = \left(A_c \ell_m\right) \int_{one\ cycle} H\, dB$$



The term $A_c \ell_m$ is the volume of the core, while the integral is the area of the B–H loop.

(energy lost per cycle) = (core volume) (area of B–H loop)

$$P_H = \left(f\right)\left(A_c \ell_m\right) \int_{one\ cycle} H\, dB$$

Hysteresis loss is directly proportional to applied frequency

Modeling hysteresis loss

- Hysteresis loss varies directly with applied frequency
- Dependence on maximum flux density: how does area of B–H loop depend on maximum flux density (and on applied waveforms)? Empirical equation (Steinmetz equation):

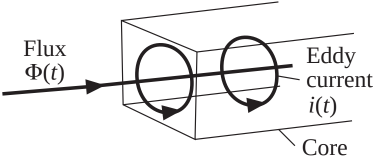
$$P_H = K_H f B_{\max}^{\alpha} (\textit{core volume})$$

The parameters K_H and α are determined experimentally.

Dependence of P_H on B_{max} is predicted by the theory of magnetic domains.

Core loss: eddy current loss

Magnetic core materials are reasonably good conductors of electric current. Hence, according to Lenz's law, magnetic fields within the core induce currents ("eddy currents") to flow within the core. The eddy currents flow such that they tend to generate a flux which opposes changes in the core flux $\Phi(t)$. The eddy currents tend to prevent flux from penetrating the core.



Eddy current loss $i^2(t)R$

Modeling eddy current loss

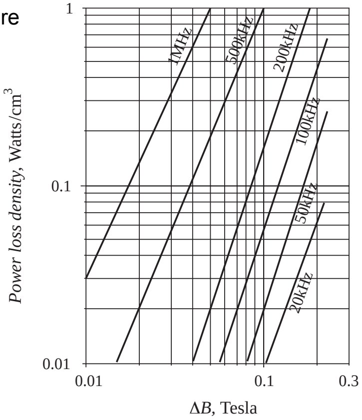
- Ac flux $\Phi(t)$ induces voltage $v(t)$ in core, according to Faraday's law. Induced voltage is proportional to derivative of $\Phi(t)$. In consequence, magnitude of induced voltage is directly proportional to excitation frequency f.
- If core material impedance Z is purely resistive and independent of frequency, $Z = R$, then eddy current magnitude is proportional to voltage: $i(t) = v(t)/R$. Hence magnitude of $i(t)$ is directly proportional to excitation frequency f.
- Eddy current power loss $i^2(t)R$ then varies with square of excitation frequency f.
- Classical Steinmetz equation for eddy current loss:

$$P_E = K_E f^2 B_{\max}^2 (\mathit{core\ volume})$$

- Ferrite core material impedance is capacitive. This causes eddy current power loss to increase as f^4.

Total core loss: manufacturer's data

Ferrite core material



Empirical equation, at a fixed frequency:

$$P_{fe} = K_{fe} (\Delta B)^{\beta} A_c \ell_m$$

Core materials

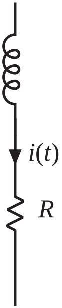
Core type	B_{sat}	Relative core loss	Applications
Laminations iron, silicon steel	1.5 - 2.0 T	high	50-60 Hz transformers, inductors
Powdered cores powdered iron, molypermalloy	0.6 - 0.8 T	medium	1 kHz transformers, 100 kHz filter inductors
Ferrite Manganese-zinc, Nickel-zinc	0.25 - 0.5 T	low	20 kHz - 1 MHz transformers, ac inductors

13.3.2 Low-frequency copper loss

DC resistance of wire

$$R = \rho \frac{\ell_b}{A_w}$$

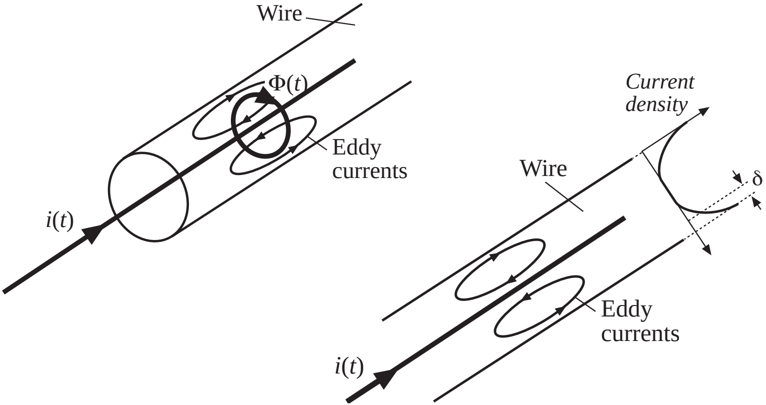
where A_w is the wire bare cross-sectional area, and ℓ_b is the length of the wire. The resistivity ρ is equal to $1.724 \cdot 10^{-6}\ \Omega\ \text{cm}$ for soft-annealed copper at room temperature. This resistivity increases to $2.3 \cdot 10^{-6}\ \Omega\ \text{cm}$ at 100°C.



The wire resistance leads to a power loss of

$$P_{cu} = I_{rms}^2 R$$

13.4 Eddy currents in winding conductors
13.4.1 Intro to the skin and proximity effects



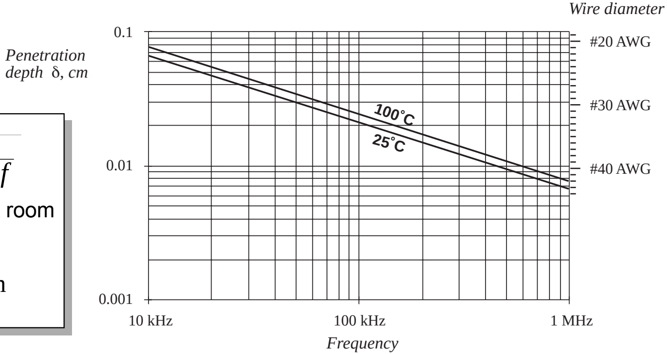
Penetration depth δ

For sinusoidal currents: current density is an exponentially decaying function of distance into the conductor, with characteristic length δ known as the *penetration depth* or *skin depth*.

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}}$$

For copper at room temperature:

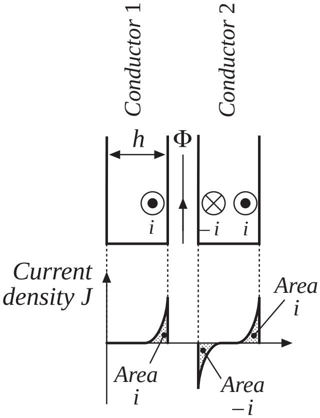
$$\delta = \frac{7.5}{\sqrt{f}} \text{ cm}$$



The proximity effect

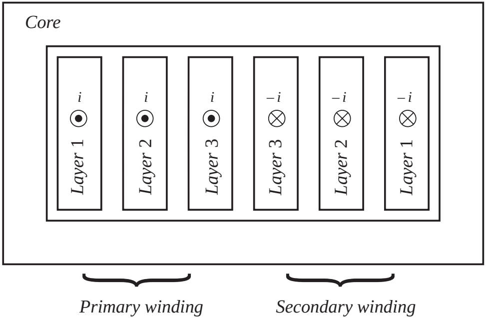
Ac current in a conductor induces eddy currents in adjacent conductors by a process called the *proximity effect*. This causes significant power loss in the windings of high-frequency transformers and ac inductors.

A multi-layer foil winding, with $h \gg \delta$. Each layer carries net current $i(t)$.



Example: a two-winding transformer

Cross-sectional view of two-winding transformer example. Primary turns are wound in three layers. For this example, let's assume that each layer is one turn of a flat foil conductor. The secondary is a similar three-layer winding. Each layer carries net current $i(t)$. Portions of the windings that lie outside of the core window are not illustrated. Each layer has thickness $h \gg \delta$.



Distribution of currents on surfaces of conductors: two-winding example

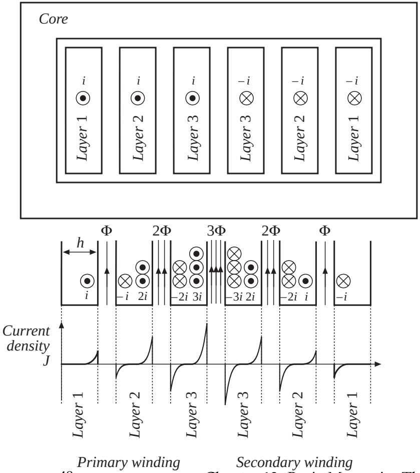
Skin effect causes currents to concentrate on surfaces of conductors

Surface current induces equal and opposite current on adjacent conductor

This induced current returns on opposite side of conductor

Net conductor current is equal to $i(t)$ for each layer, since layers are connected in series

Circulating currents within layers increase with the numbers of layers



Estimating proximity loss: high-frequency limit

The current $i(t)$ having rms value I is confined to thickness d on the surface of layer 1. Hence the effective "ac" resistance of layer 1 is:

$$R_{ac} = \frac{h}{\delta} R_{dc}$$

This induces copper loss P_1 in layer 1:

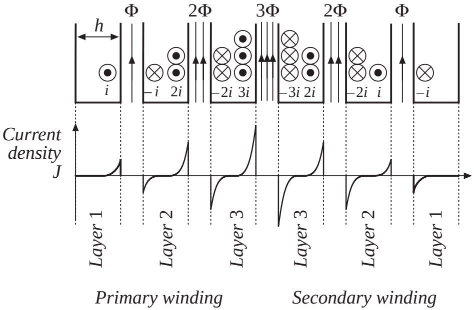
$$P_1 = I^2 R_{ac}$$

Power loss P_2 in layer 2 is:

$$P_2 = P_1 + 4P_1 = 5P_1$$

Power loss P_3 in layer 3 is:

$$P_3 = \left(2^2 + 3^2\right) P_1 = 13 P_1$$



Power loss P_m in layer m is:

$$P_m = I^2 \left[(m-1)^2 + m^2 \right] \left(\frac{h}{\delta} R_{dc} \right)$$

Total loss in M-layer winding: high-frequency limit

Add up losses in each layer:

$$P = I^2 \left(\frac{h}{\delta} R_{dc} \right) \sum_{m=1}^{M} \left[\left(m-1 \right)^2 + m^2 \right]$$
$$= I^2 \left(\frac{h}{\delta} R_{dc} \right) \frac{M}{3} \left(2M^2 + 1 \right)$$

Compare with dc copper loss:

If foil thickness were $H = \delta$, then at dc each layer would produce copper loss P_1. The copper loss of the M-layer winding would be

$$P_{dc} = I^2 M R_{dc}$$

So the proximity effect increases the copper loss by a factor of

$$F_R = \frac{P}{P_{dc}} = \frac{1}{3} \left(\frac{h}{\delta} \right) \left(2M^2 + 1 \right)$$

Discussion: design of winding geometry to minimize proximity loss

- Interleaving windings can significantly reduce the proximity loss when the winding currents are in phase, such as in the transformers of buck-derived converters or other converters
- In some converters (such as flyback or SEPIC) the winding currents are out of phase. Interleaving then does little to reduce the peak MMF and proximity loss. See *Vandelac and Ziogas* [10].
- For sinusoidal winding currents, there is an optimal conductor thickness near $\varphi = 1$ that minimizes copper loss.
- Minimize the number of layers. Use a core geometry that maximizes the width ℓ_w of windings.
- Minimize the amount of copper in vicinity of high MMF portions of the windings

Litz wire

- A way to increase conductor area while maintaining low proximity losses
- Many strands of small-gauge wire are bundled together and are externally connected in parallel
- Strands are twisted, or transposed, so that each strand passes equally through each position on inside and outside of bundle. This prevents circulation of currents between strands.
- Strand diameter should be sufficiently smaller than skin depth
- The Litz wire bundle itself is composed of multiple layers
- Advantage: when properly sized, can significantly reduce proximity loss
- Disadvantage: increased cost and decreased amount of copper within core window

Practical realisations and simulations

- Transformer (50 Hz)
- Transformer (20 kHz)
- Inductors
- Simulations with ONELAB

Introduction to Resonant Conversion

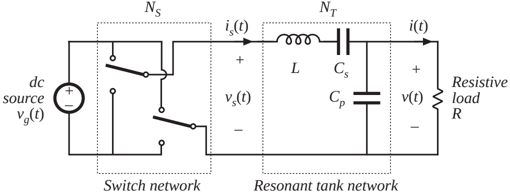
Resonant power converters contain resonant L-C networks whose voltage and current waveforms vary sinusoidally during one or more subintervals of each switching period. These sinusoidal variations are large in magnitude, and the small ripple approximation does not apply.

Some types of resonant converters:

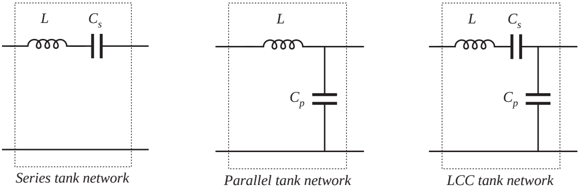
- Dc-to-high-frequency-ac inverters
- Resonant dc-dc converters
- Resonant inverters or rectifiers producing line-frequency ac

A basic class of resonant inverters

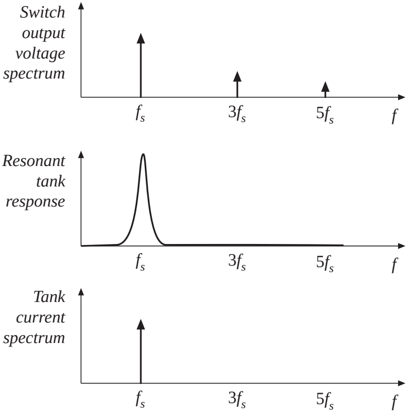
Basic circuit



Several resonant tank networks



Tank network responds only to fundamental component of switched waveforms

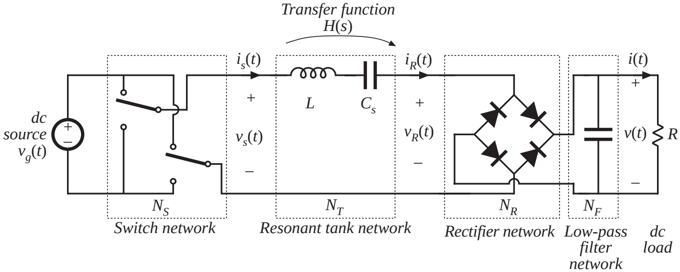


Tank current and output voltage are essentially sinusoids at the switching frequency f_s.

Output can be controlled by variation of switching frequency, closer to or away from the tank resonant frequency

Derivation of a resonant dc-dc converter

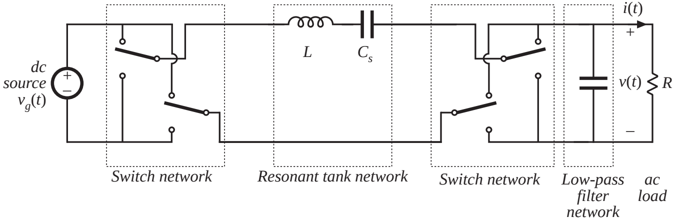
Rectify and filter the output of a dc-high-frequency-ac inverter



The series resonant dc-dc converter

A series resonant link inverter

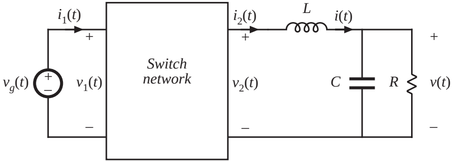
Same as dc-dc series resonant converter, except output rectifiers are replaced with four-quadrant switches:



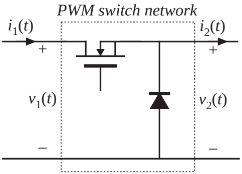
Quasi-resonant converters

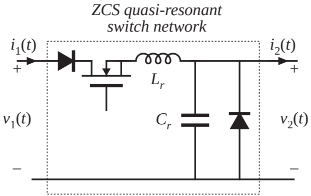
In a conventional PWM converter, replace the PWM switch network with a switch network containing resonant elements.

Buck converter example



Two switch networks:





Resonant conversion: advantages

The chief advantage of resonant converters: reduced switching loss

Zero-current switching

Zero-voltage switching

Turn-on or turn-off transitions of semiconductor devices can occur at zero crossings of tank voltage or current waveforms, thereby reducing or eliminating some of the switching loss mechanisms. Hence resonant converters can operate at higher switching frequencies than comparable PWM converters

Zero-voltage switching also reduces converter-generated EMI

Zero-current switching can be used to commutate SCRs

In specialized applications, resonant networks may be unavoidable

High voltage converters: significant transformer leakage inductance and winding capacitance leads to resonant network

Resonant conversion: disadvantages

Can optimize performance at one operating point, but not with wide range of input voltage and load power variations

Significant currents may circulate through the tank elements, even when the load is disconnected, leading to poor efficiency at light load

Quasi-sinusoidal waveforms exhibit higher peak values than equivalent rectangular waveforms

These considerations lead to increased conduction losses, which can offset the reduction in switching loss

Resonant converters are usually controlled by variation of switching frequency. In some schemes, the range of switching frequencies can be very large

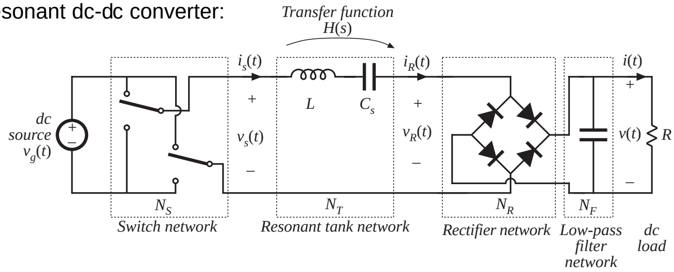
Complexity of analysis

Resonant conversion: Outline of discussion

- Simple steady-state analysis via sinusoidal approximation
- Simple and exact results for the series and parallel resonant converters
- Mechanisms of soft switching
- Circulating currents, and the dependence (or lack thereof) of conduction loss on load power
- Quasi-resonant converter topologies
- Steady-state analysis of quasi-resonant converters
- Ac modeling of quasi-resonant converters via averaged switch modeling

19.1 Sinusoidal analysis of resonant converters

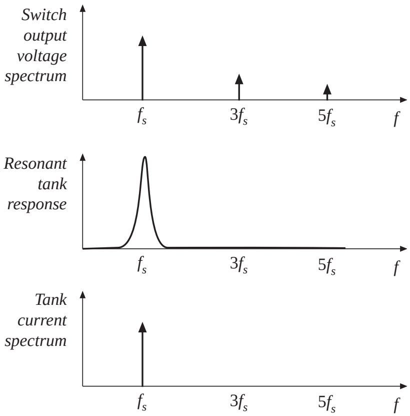
A resonant dc-dc converter:



If tank responds primarily to fundamental component of switch network output voltage waveform, then harmonics can be neglected.

Let us model all ac waveforms by their fundamental components.

The sinusoidal approximation

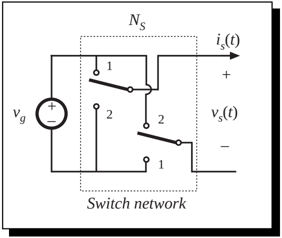


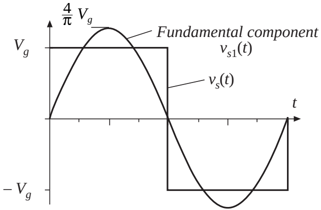
Tank current and output voltage are essentially sinusoids at the switching frequency f_s.

Neglect harmonics of switch output voltage waveform, and model only the fundamental component.

Remaining ac waveforms can be found via phasor analysis.

19.1.1 Controlled switch network model





If the switch network produces a square wave, then its output voltage has the following Fourier series:

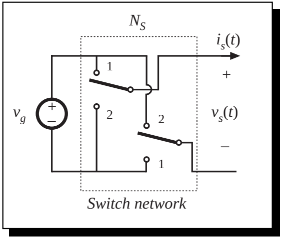
$$v_s(t) = \frac{4V_g}{\pi} \sum_{n=1,3,5,...} \frac{1}{n} \sin(n\omega_s t)$$

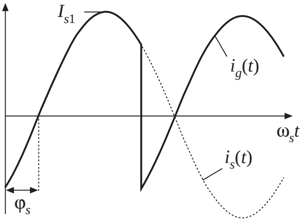
The fundamental component is

$$v_{s1}(t) = \frac{4V_g}{\pi} \sin(\omega_s t) = V_{s1} \sin(\omega_s t)$$

So model switch network output port with voltage source of value $v_{s1}(t)$

Model of switch network input port





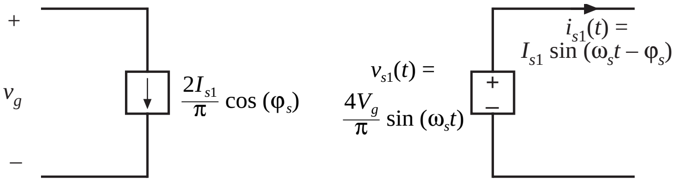
Assume that switch network output current is

$$i_s(t) \approx I_{s1} \sin(\omega_s t - \varphi_s)$$

It is desired to model the dc component (average value) of the switch network input current.

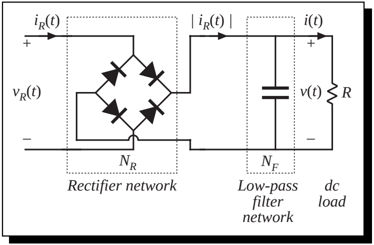
$$\begin{aligned} \left\langle i_g(t) \right\rangle_{T_s} &= \frac{2}{T_s} \int_0^{T_s/2} i_g(\tau) d\tau \\ &\approx \frac{2}{T_s} \int_0^{T_s/2} I_{s1} \sin(\omega_s \tau - \varphi_s) d\tau \\ &= \frac{2}{\pi} I_{s1} \cos(\varphi_s) \end{aligned}$$

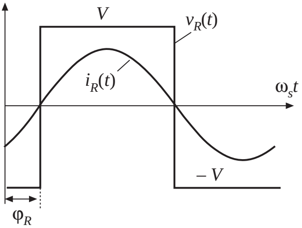
Switch network: equivalent circuit



- Switch network converts dc to ac
- Dc components of input port waveforms are modeled
- Fundamental ac components of output port waveforms are modeled
- Model is power conservative: predicted average input and output powers are equal

19.1.2 Modeling the rectifier and capacitive filter networks





Assume large output filter capacitor, having small ripple.

$v_R(t)$ is a square wave, having zero crossings in phase with tank output current $i_R(t)$.

If $i_R(t)$ is a sinusoid:

$$i_R(t) = I_{R1} \sin(\omega_s t - \varphi_R)$$

Then $v_R(t)$ has the following Fourier series:

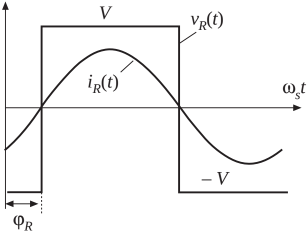
$$v_R(t) = \frac{4V}{\pi} \sum_{n=1,3,5,\cdots}^{\infty} \frac{1}{n} \sin(n\omega_s t - \varphi_R)$$

Sinusoidal approximation: rectifier

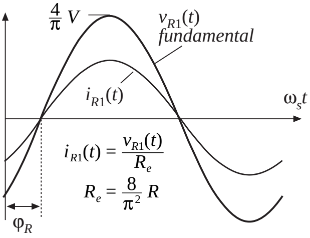
Again, since tank responds only to fundamental components of applied waveforms, harmonics in $v_R(t)$ can be neglected. $v_R(t)$ becomes

$$v_{R1}(t) = \frac{4V}{\pi} \sin(\omega_s t - \varphi_R) = V_{R1} \sin(\omega_s t - \varphi_R)$$

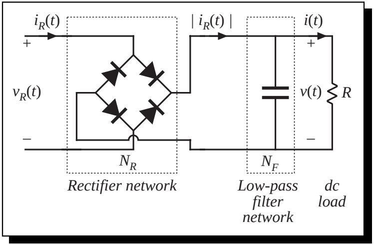
Actual waveforms

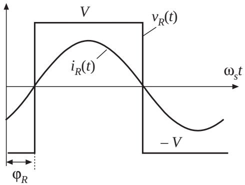


with harmonics ignored



Rectifier dc output port model





Output capacitor charge balance: dc load current is equal to average rectified tank output current

$$\left\langle \left| i_R(t) \right| \right\rangle_{T_s} = I$$

Hence

$$I = \frac{2}{T_S} \int_0^{T_s/2} I_{R1} \left| \sin\left(\omega_s t - \varphi_R\right) \right| dt$$
$$= \frac{2}{\pi} I_{R1}$$

Equivalent circuit of rectifier

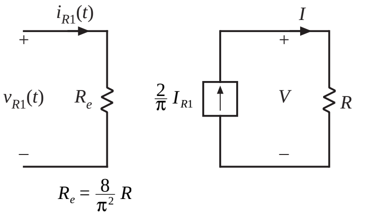
Rectifier input port:

Fundamental components of current and voltage are sinusoids that are in phase

Hence rectifier presents a resistive load to tank network

Effective resistance R_e is

$$R_e = \frac{v_{R1}(t)}{i_R(t)} = \frac{8}{\pi^2}\frac{V}{I}$$

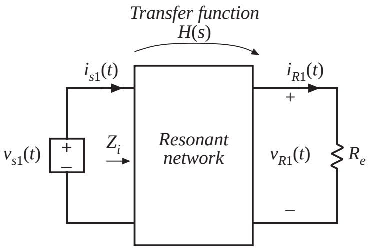


Rectifier equivalent circuit

With a resistive load R, this becomes

$$R_e = \frac{8}{\pi^2} R = 0.8106R$$

19.1.3 Resonant tank network



Model of ac waveforms is now reduced to a linear circuit. Tank network is excited by effective sinusoidal voltage (switch network output port), and is load by effective resistive load (rectifier input port).

Can solve for transfer function via conventional linear circuit analysis.

Solution of tank network waveforms

Transfer function:

$$\frac{v_{R1}(s)}{v_{s1}(s)} = H(s)$$

Ratio of peak values of input and output voltages:

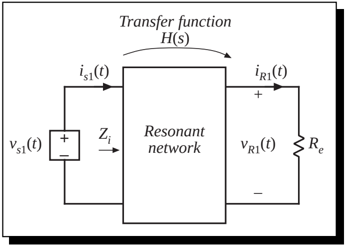
$$\frac{V_{R1}}{V_{s1}} = \left\| H(s) \right\|_{s = j\omega_s}$$

Solution for tank output current:

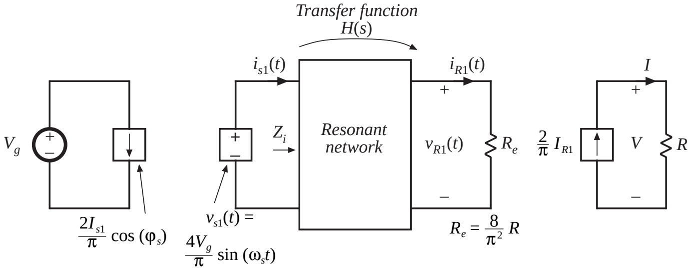
$$i_R(s) = \frac{v_{R1}(s)}{R_e} = \frac{H(s)}{R_e}\, v_{s1}(s)$$

which has peak magnitude

$$I_{R1} = \frac{\left\| H(s) \right\|_{s = j\omega_s}}{R_e}\, V_{s1}$$



19.1.4 Solution of converter voltage conversion ratio $M = V/V_g$



$$M = \frac{V}{V_g} = \underbrace{\left(R\right)}_{\left(\frac{V}{I}\right)} \underbrace{\left(\frac{2}{\pi}\right)}_{\left(\frac{I}{I_{R1}}\right)} \underbrace{\left(\frac{1}{R_e}\right)}_{\left(\frac{I_{R1}}{V_{R1}}\right)} \underbrace{\left(\left\| H(s) \right\|_{s = j\omega_s}\right)}_{\left(\frac{V_{R1}}{V_{s1}}\right)} \underbrace{\left(\frac{4}{\pi}\right)}_{\left(\frac{V_{s1}}{V_g}\right)}$$

Eliminate R_e:

$$\frac{V}{V_g} = \left\| H(s) \right\|_{s = j\omega_s}$$

Conversion ratio M

$$\frac{V}{V_g} = \left\| H(s) \right\|_{s = j\omega_s}$$

So we have shown that the conversion ratio of a resonant converter, having switch and rectifier networks as in previous slides, is equal to the magnitude of the tank network transfer function. This transfer function is evaluated with the tank loaded by the effective rectifier input resistance R_e.

19.4 Soft switching

Soft switching can mitigate some of the mechanisms of switching loss and possibly reduce the generation of EMI

Semiconductor devices are switched on or off at the zero crossing of their voltage or current waveforms:

Zero-current switching: transistor turn-off transition occurs at zero current. Zero-current switching eliminates the switching loss caused by IGBT current tailing and by stray inductances. It can also be used to commutate SCR's.

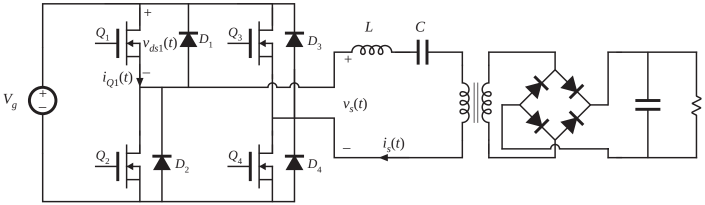
Zero-voltage switching: transistor turn-on transition occurs at zero voltage. Diodes may also operate with zero-voltage switching. Zero-voltage switching eliminates the switching loss induced by diode stored charge and device output capacitances.

Zero-voltage switching is usually preferred in modern converters.

Zero-voltage transition converters are modified PWM converters, in which an inductor charges and discharges the device capacitances. Zero-voltage switching is then obtained.

19.4.1 Operation of the full bridge below resonance: Zero-current switching

Series resonant converter example



Operation below resonance: input tank current leads voltage

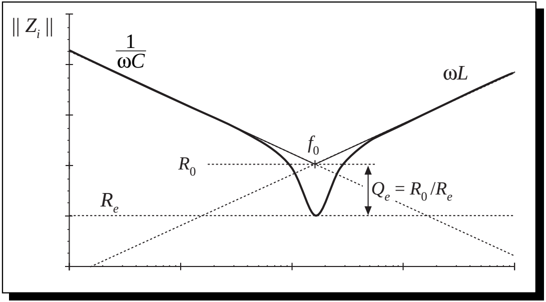
Zero-current switching (ZCS) occurs

Tank input impedance

Operation below resonance: tank input impedance Z_i is dominated by tank capacitor.

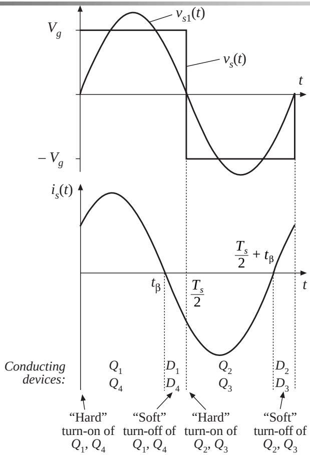
$\angle Z_i$ is positive, and tank input current leads tank input voltage.

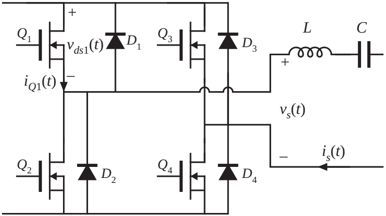
Zero crossing of the tank input current waveform $i_s(t)$ occurs before the zero crossing of the voltage $v_s(t)$.



Switch network waveforms, below resonance

Zero-current switching

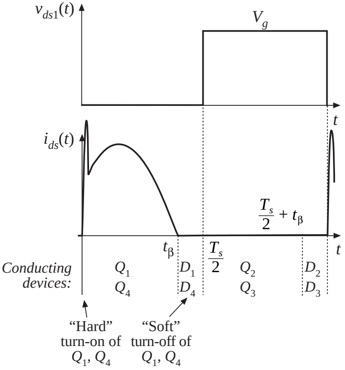


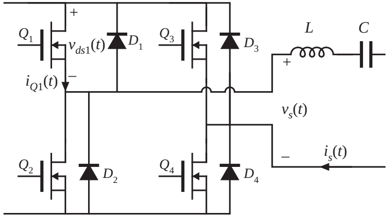


Conduction sequence: Q_1–D_1–Q_2–D_2

Q_1 is turned off during D_1 conduction interval, without loss

ZCS turn-on transition: hard switching

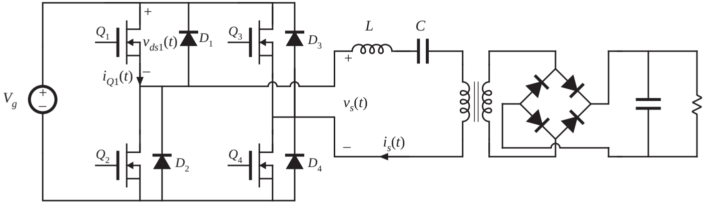




Q_1 turns on while D_2 is conducting. Stored charge of D_2 and of semiconductor output capacitances must be removed. Transistor turn-on transition is identical to hard-switched PWM, and switching loss occurs.

19.4.2 Operation of the full bridge below resonance: Zero-voltage switching

Series resonant converter example



Operation above resonance: input tank current lags voltage

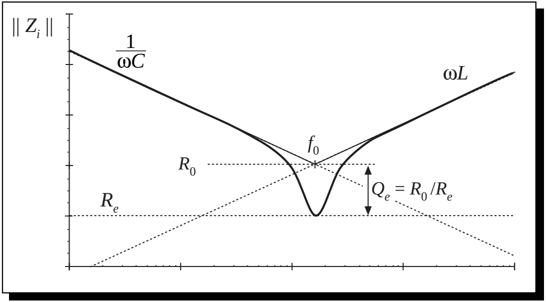
Zero-voltage switching (ZVS) occurs

Tank input impedance

Operation above resonance: tank input impedance Z_i is dominated by tank inductor.

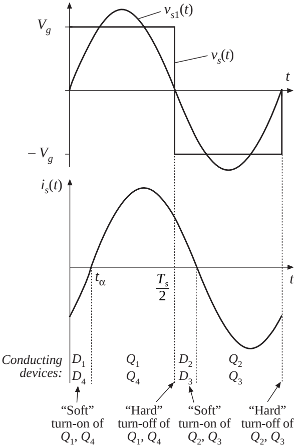
$\angle Z_i$ is negative, and tank input current lags tank input voltage.

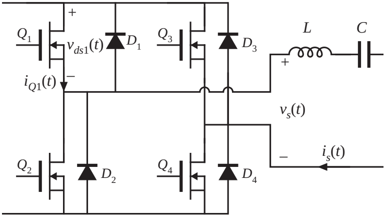
Zero crossing of the tank input current waveform $i_s(t)$ occurs after the zero crossing of the voltage $v_s(t)$.



Switch network waveforms, above resonance

Zero-voltage switching

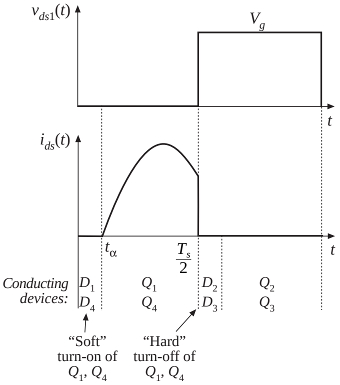


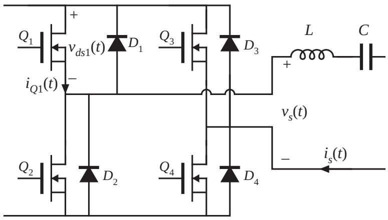


Conduction sequence: D_1–Q_1–D_2–Q_2

Q_1 is turned on during D_1 conduction interval, without loss

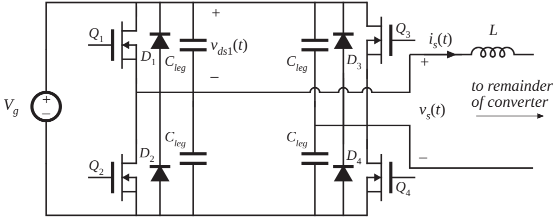
ZVS turn-off transition: hard switching?



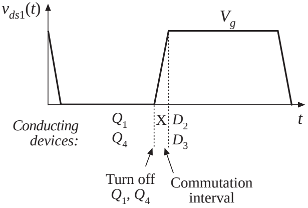


When Q_1 turns off, D_2 must begin conducting. Voltage across Q_1 must increase to V_g. Transistor turn-off transition is identical to hard-switched PWM. Switching loss may occur (but see next slide).

Soft switching at the ZVS turn-off transition



- Introduce small capacitors C_{leg} across each device (or use device output capacitances).
- Introduce delay between turn-off of Q_1 and turn-on of Q_2.

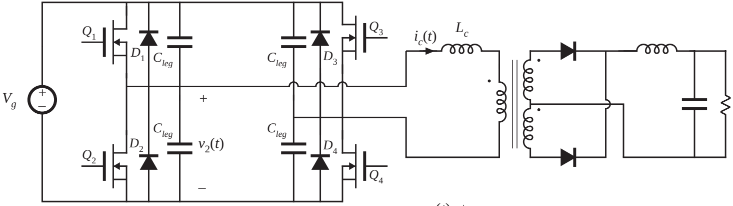


Tank current $i_s(t)$ charges and discharges C_{leg}. Turn-off transition becomes lossless. During commutation interval, no devices conduct.

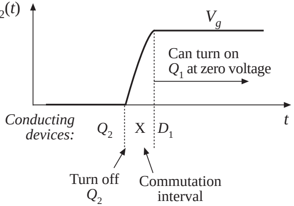
So zero-voltage switching exhibits low switching loss: losses due to diode stored charge and device output capacitances are eliminated.

19.4.3 The zero-voltage transition converter

Basic version based on full-bridge PWM buck converter



- Can obtain ZVS of all primary-side MOSFETs and diodes
- Secondary-side diodes switch at zero-current, with loss
- Phase-shift control



19.5 Load-dependent properties of resonant converters

Resonant inverter design objectives:

1. Operate with a specified load characteristic and range of operating points
   - With a nonlinear load, must properly match inverter output characteristic to load characteristic
2. Obtain zero-voltage switching or zero-current switching
   - Preferably, obtain these properties at all loads
   - Could allow ZVS property to be lost at light load, if necessary
3. Minimize transistor currents and conduction losses
   - To obtain good efficiency at light load, the transistor current should scale proportionally to load current (in resonant converters, it often doesn't!)

References I

[1] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*.
Kluwer Academic Publishers, second ed., 2001.

[2] P. M. Luca Corradini, Dragan Maksimović and R. Zane, *Digital Control of High-Frequency Switched-Mode Power Converters*.
Wiley-IEEE Press, 2015.

[3] R. W. Erickson and D. Maksimović, "Fundamentals of power electronics slides: http://ecee.colorado.edu/copec/book/slides/slidedir.html," 2001.

[4] Mohan, Undeland, and Robbins, *POWER ELECTRONICS: Converters, Applications and Design*.
Wiley, third ed., 2003.