Design rules
For electronic circuits and PCBs
(part III)

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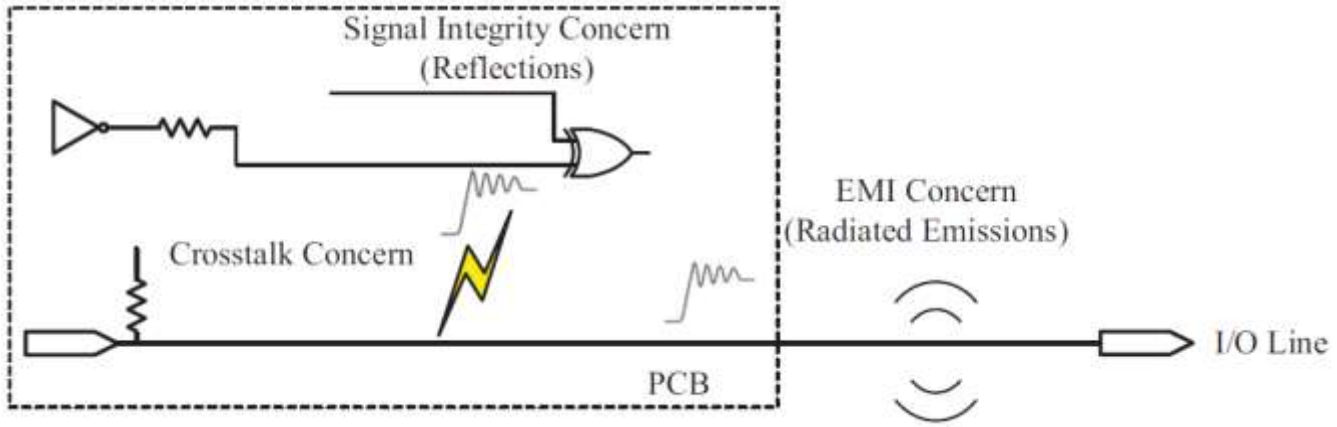
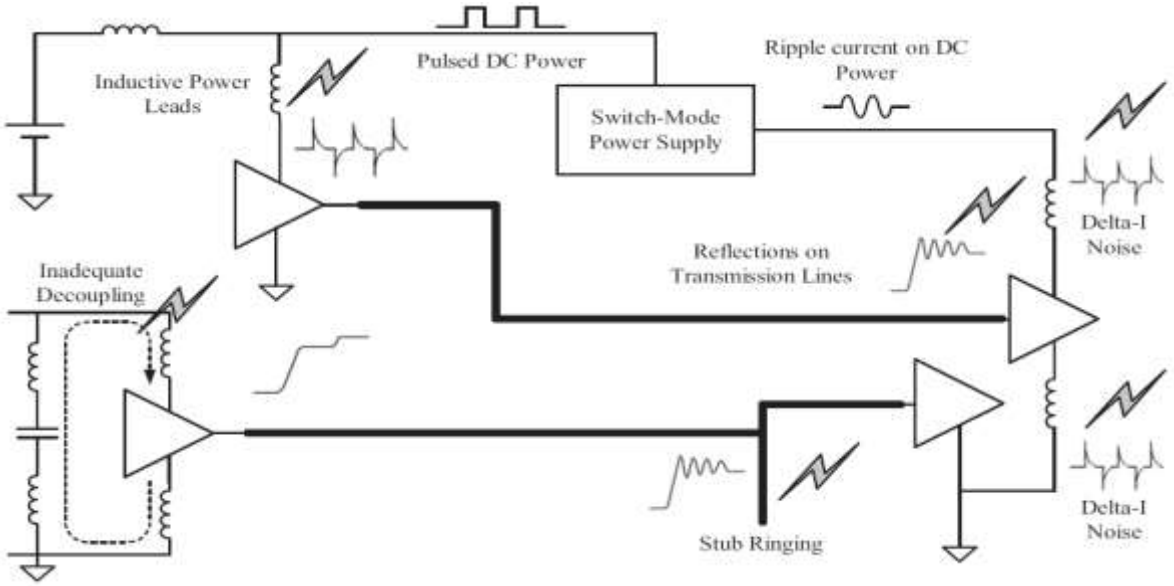
9.1 Interference sources on PCBs

- Studies have shown that VLSI devices (processor, DDR memories, FPGA) are to small to act as direct sources of radiated EMI but,
- EMI noise is generated by:
  - coupling to heatsink,
  - coupling to traces,
  - coupling to reference plane.



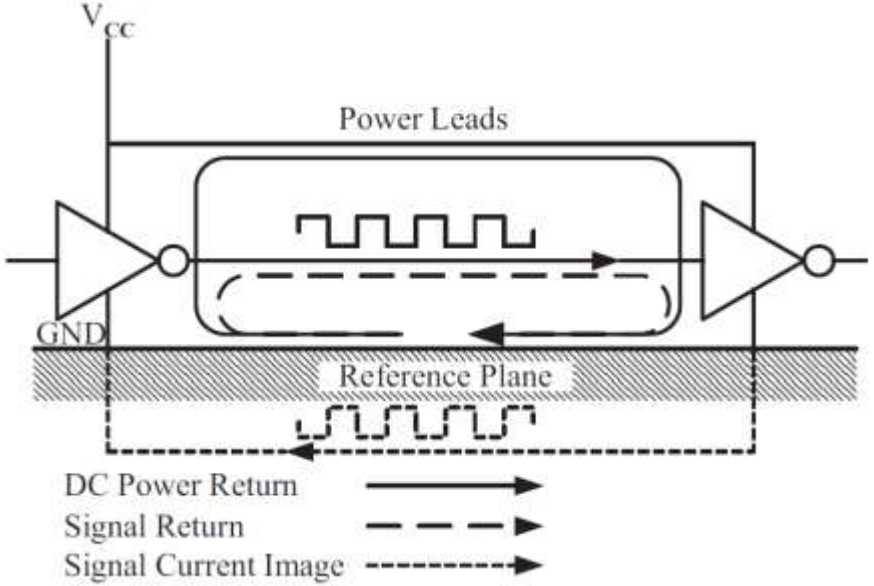
9.1 Interference sources on PCBs

- Common-impedance coupling through power supplies,
- Common-impedance coupling through return conductor,
- Mismatch on high-speed transmission lines -> reflections,
- Crosstalk coupling between adjacent conductors of different circuits,
- Coupling in low level, high gain amplifiers,
- Transients from inductive load switching, coupling to adjacent circuits,
- Power-supply-generated-noise entering sensitive circuits.

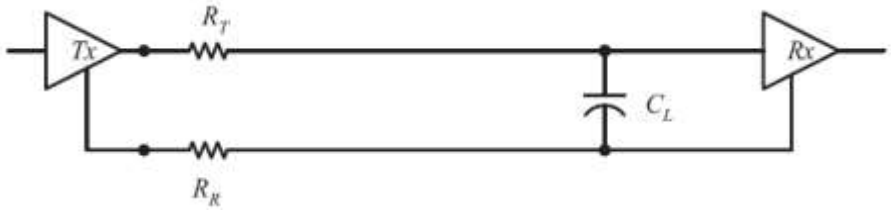


9.2 ”Grounding” on PCBs

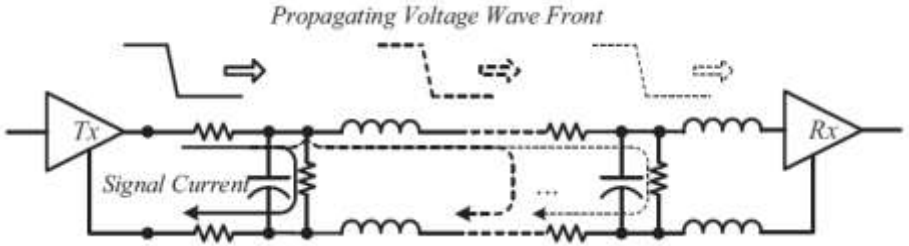
- What are the functions of “grounding” on a PCB ?
  - **Signal return path**. For each high-speed digital signal, a current goes from the source to the destination, the return current need a path that is provided by the ground.
  - **DC power return path.** Power DC supply current goes back to the power DC supply through the ground plane.
  - **Image plane.** By providing a ground plane close to signal layers, the ground plane provides an image plane that allows image currents to flow, therefore reducing EMI.



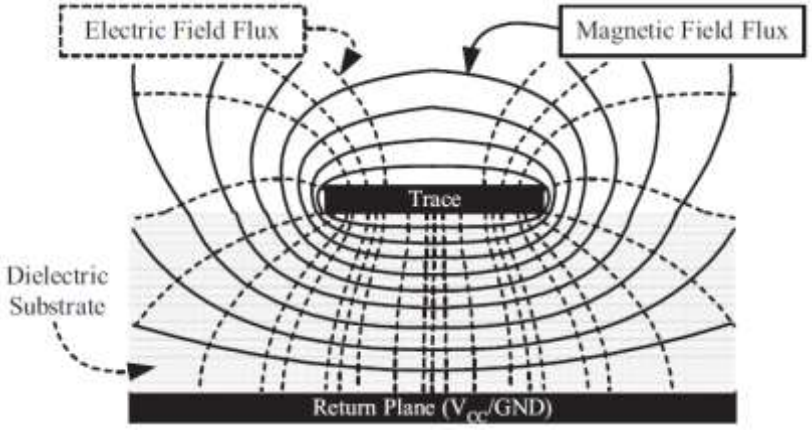
9.3 Signal propagation on PCBs



Lumped representation (LF)



Signal propagation (HF)

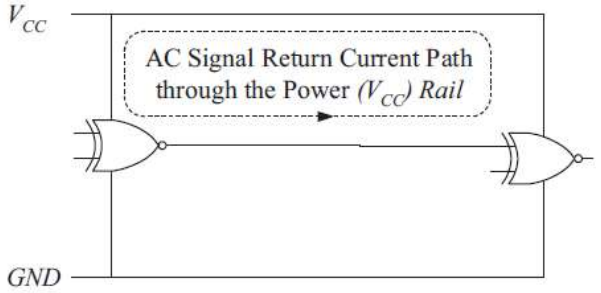


Field representation (TEM)

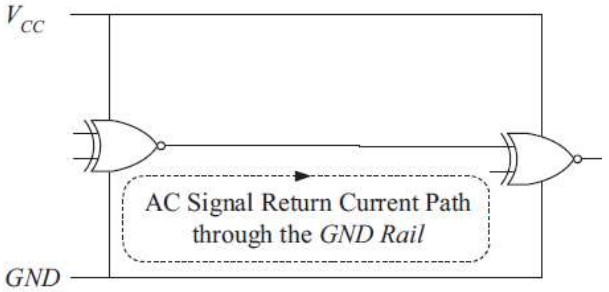
- Signal propagation involves important aspects to be managed (undesired TL effects): **ringing, crosstalk, reflection and ground bounce.**
- These aspects have to be managed by controlling impedance and by applying simple design guidelines that will be explained.

9.3.3 Equivalence of return path

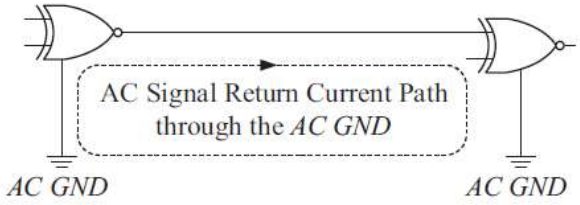
- Current in the signal line has to come back.
- Any power rail can be used as return path.
- The power rail with minimum inductance will drain the return current.



(a) Return RF Current Flow through V_{CC}



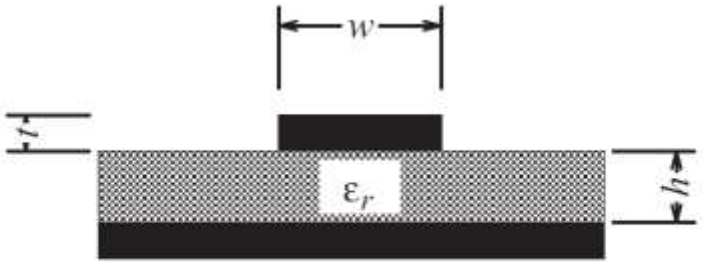
(b) Return RF Current Flow through GND



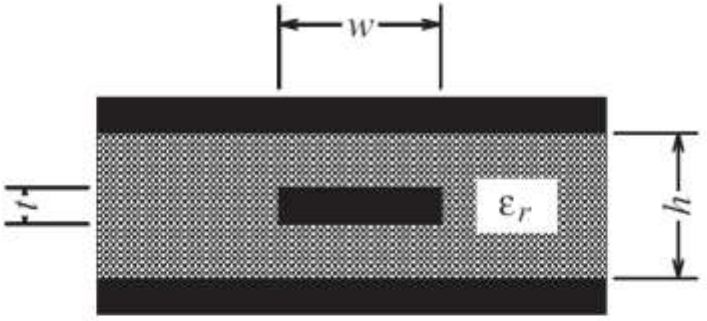
(c) Return RF Current Flow through AC GND

9.3.4 Single-ended transmission lines

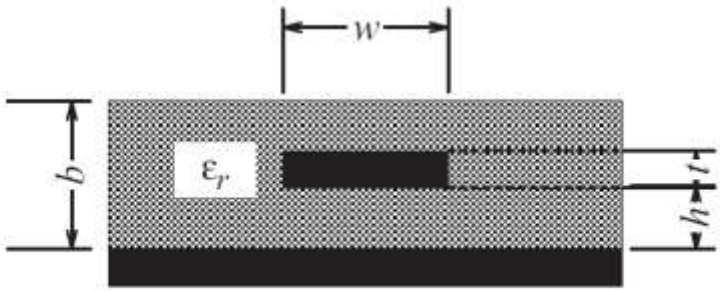
- Microstrip (left) transmission lines impedance is less sensitive to ε_r, losses are minimized.
- Stripline (right) transmission lines minimize crosstalk and EMI.



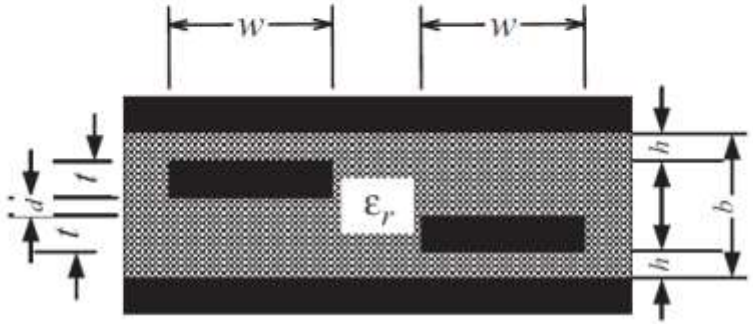
(a) Geometry of a Surface Microstrip Transmission Line



(a) Geometry of a Centered Stripline Transmission Line



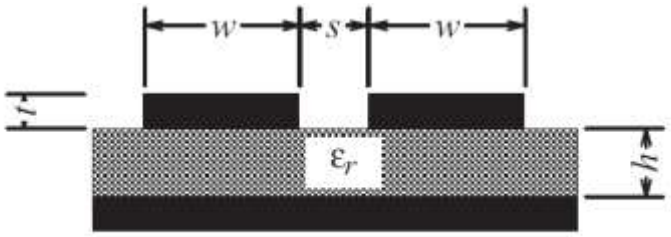
(b) Geometry of a Embedded Microstrip Transmission Line



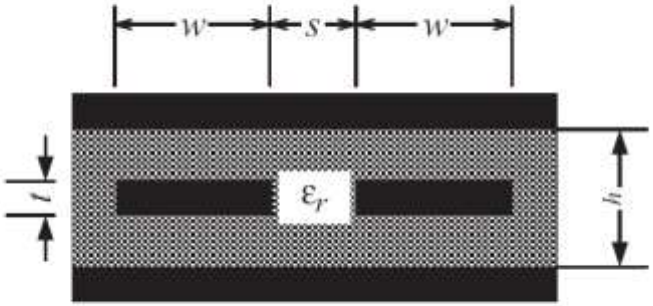
(b) Geometry of a Dual Stripline Transmission Line

9.3.4 Differential transmission lines

- Same considerations apply for differential lines compared to single-ended.



(a) Geometry of a Differential Edge Coupled Microstrip Transmission Line



(b) Geometry of a Differential Edge Coupled Stripline Transmission Line

- Broadside transmission lines are useful in backplane design because they are easier to route through high density connectors.

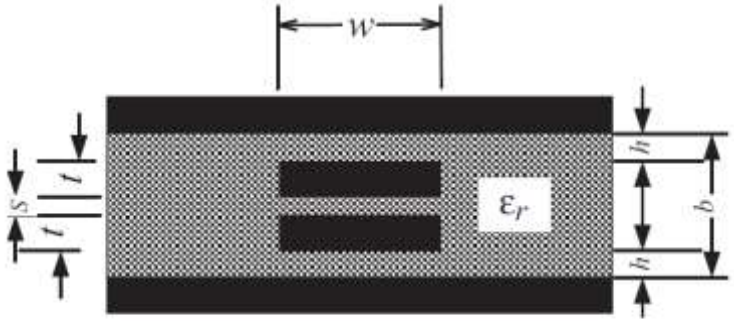


Figure 9.15. Geometry of broadside coupled stripline.

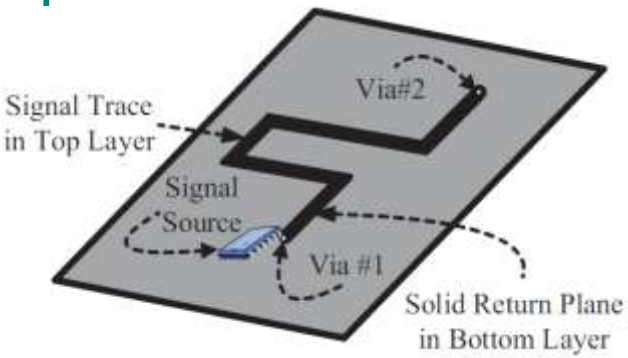
9.3.4 Transmission lines

- Z_0 and Z_{DIFF} formulae can be found in [1] page 639 to page 645.

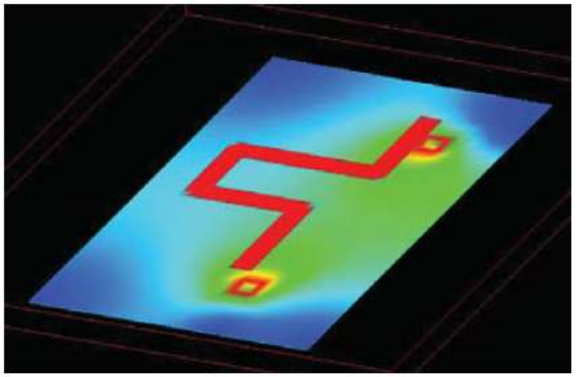
- Take care of definition:Definitions of impedance related terms:
  - ✓ Single ended Zo: The impedance seen when testing a single line which is not coupled to an adjacent line
  - ✓ Differential (Zdiff): The impedance testing between a pair of lines when driven by equal and opposite polarity signals. (Zdiff is twice the value of the odd mode impedance)
  - ✓ Odd Mode (Zoo): the impedance seen when testing the impedance of one side of a pair of lines when the other is drive in equal and opposite polarity (half the value of the differential impedance)
  - ✓ Common (Zcm): The impedance seen when testing into a pair of lines driven by identical (common) signals
  - ✓ Even mode (Zoe): The impedance measured testing one of a pair of lines which are driven by identical signals (Even mode is twice the common mode value.)

More details can be found on the Polar Web site:
https://www.polarinstruments.com/support/cits/AP157.html

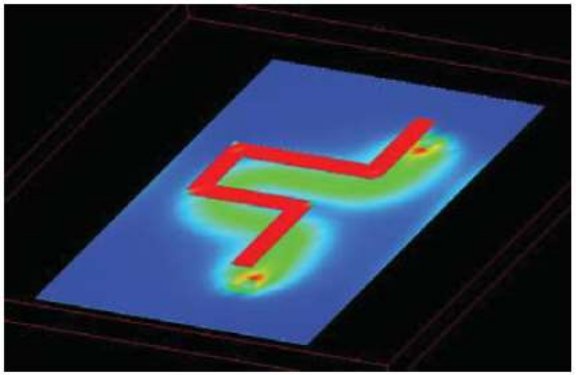
9.3.5 Return current path on PCB



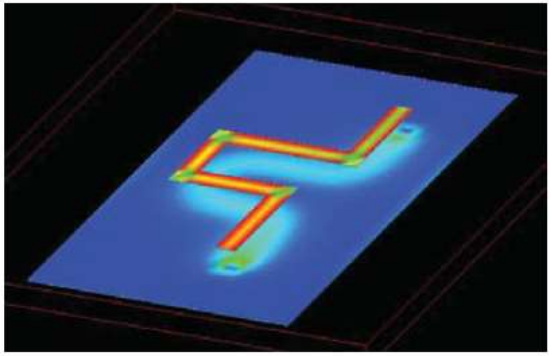
- Return current path depends on frequency!
- This can create edge distortion.
- Return current runs below the transmission line in the ground plane as soon as frequency is higher than a few MHz.
- DC return current spreads over the ground plane (a).



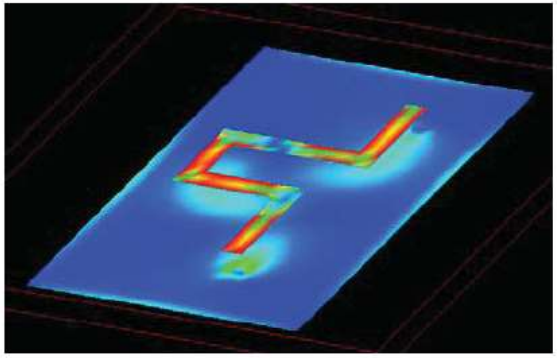
(a) Frequency of 1 kHz



(b) Frequency of 1 MHz

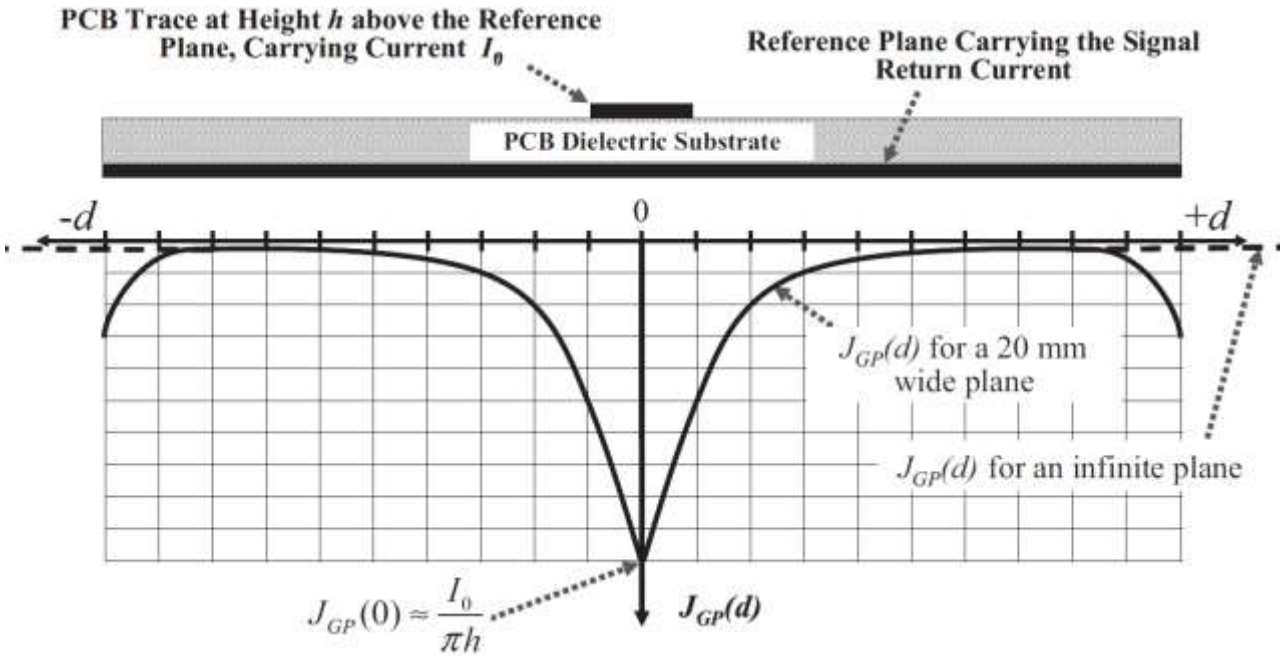


(c) Frequency of 1 GHz



(d) Frequency of 10 GHz

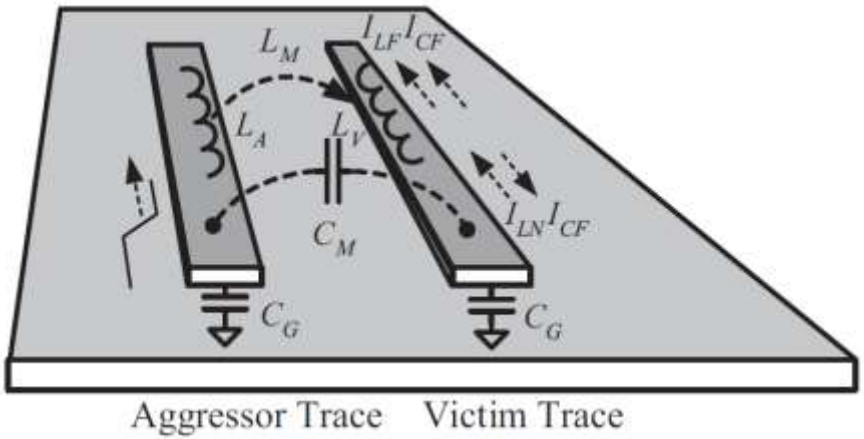
9.3.5 Return current path on PCB



- The above graph represents the current density distribution as a function of the position.
- Current density decreases quickly with d/h and can be expressed as:

$$J(d) \approx \frac{I_0}{\pi h} \cdot \frac{1}{1+(d/h)^2} \quad \text{(A/m)}$$

9.3.7 Crosstalk mechanisms on PCBs



- In digital circuits, inductive coupling is predominant due to the low impedance nature of drivers and lines.
- In analog circuits (high impedance), capacitive coupling is predominant.
- In power supplies, both coupling are present depending on the voltage and current levels.

- $I_c = C_M.dV_s/dt$. $V_L = -L_M.dI_s/dt$

- When a signal travels on the **aggressor** trace, it couples to the **victim** trace:
  - ✓ capacitive and inductive coupling reinforce in the **backward** direction (near-end crosstalk – NEXT),
  - ✓ capacitive and inductive coupling tend to cancel in the **forward** direction (far-end crosstalk – FEXT).

9.3.8 Common mode impedance coupling

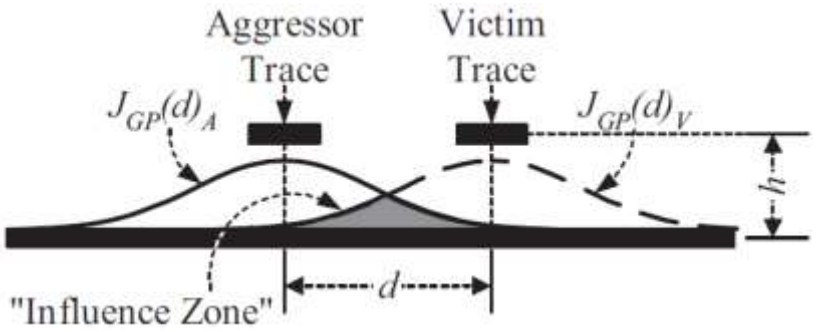
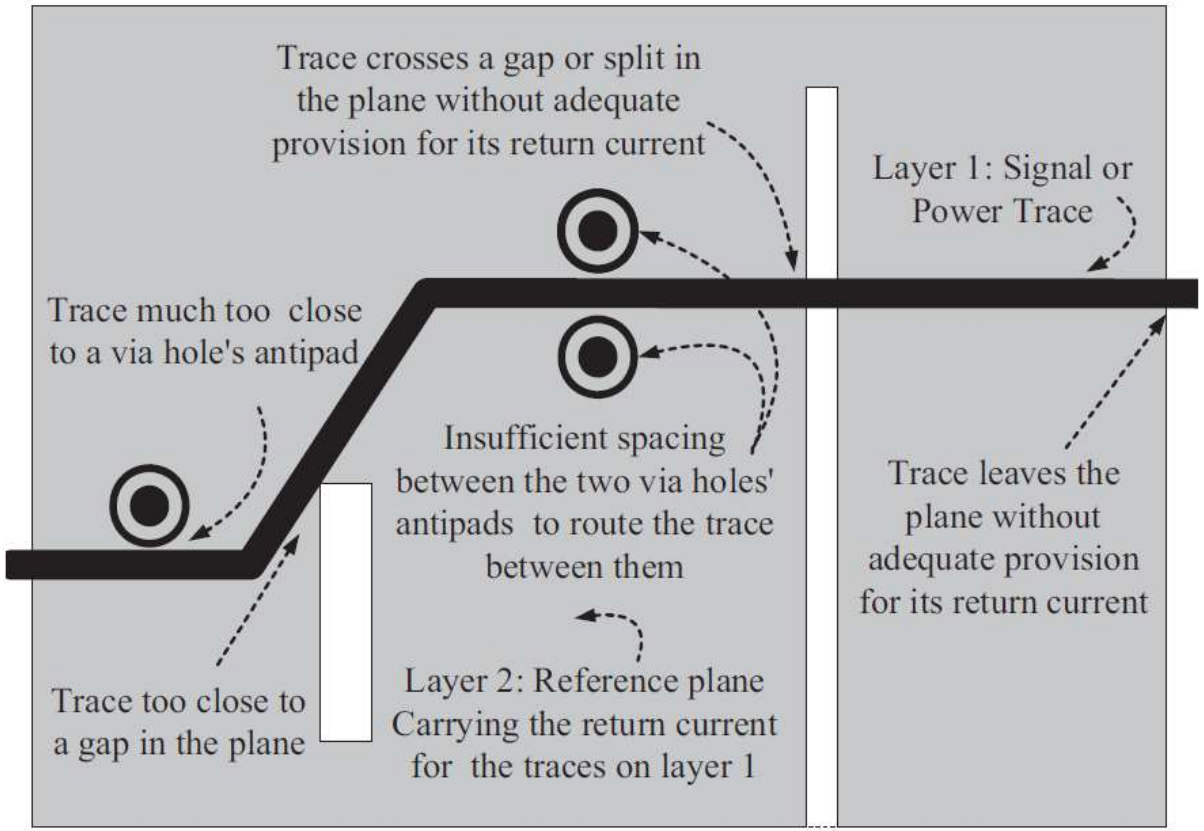


Table 9.1. Fraction (in percent) of the return current contained within a normalized distance of ±*d*/*h* from the signal trace centerline

d/*h*	Fraction of cumulative current density at distance, *d* from aggressor trace centerline (%)
2	70%
5	87%
10	94%
20	97%

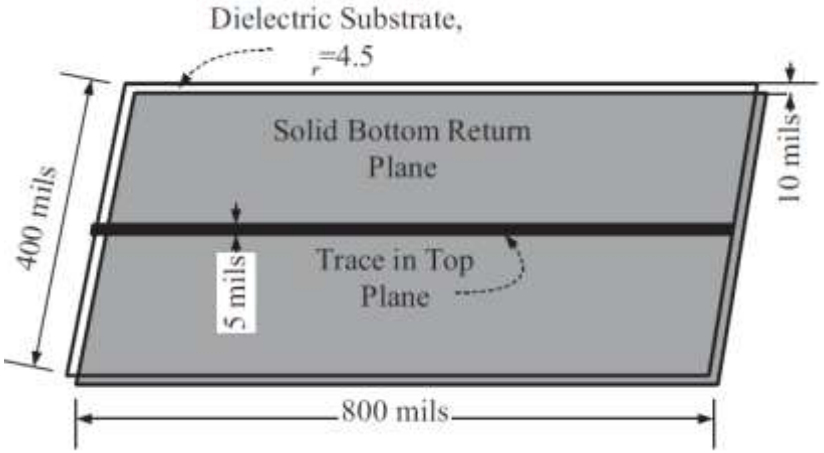
- Example:
  - ✓ A processor draws a current of 10 A in a trace.
  - ✓ An analog circuit 24-bit A/D converter with a ref of 1 V has a resolution of 5.9 nV.
  - ✓ The ground plane has a typical impedance of 40 μΩ.
  - ✓ => the acceptable ground plane current near the ADC is therefore 5.9 nV / 40 μΩ = 0.15 mA.
  - ✓ That means that only 0.15 % of the processor current can pass near the ADC, d/h has to be higher than 20.
- **Split planes** are used to avoid common impedance coupling through ground.

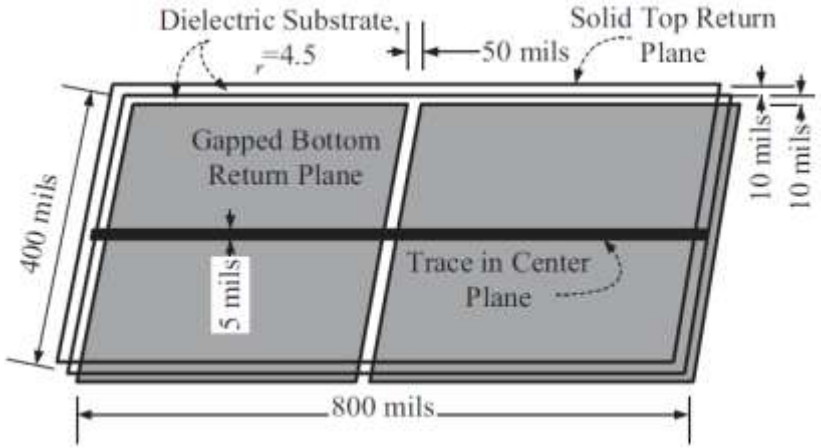
9.4. Return path discontinuities on PCBs

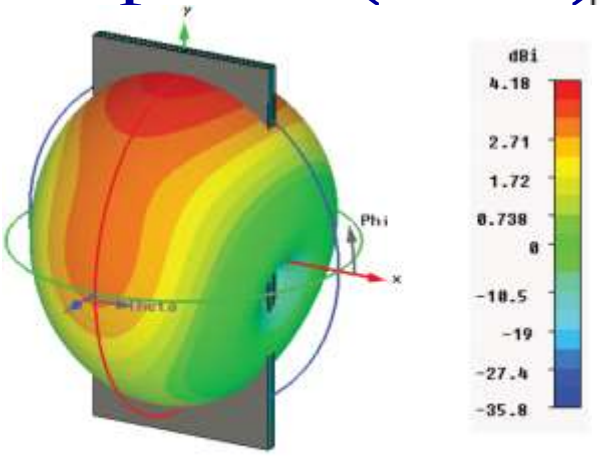


[Keith Amstrong, Cherry Clough]

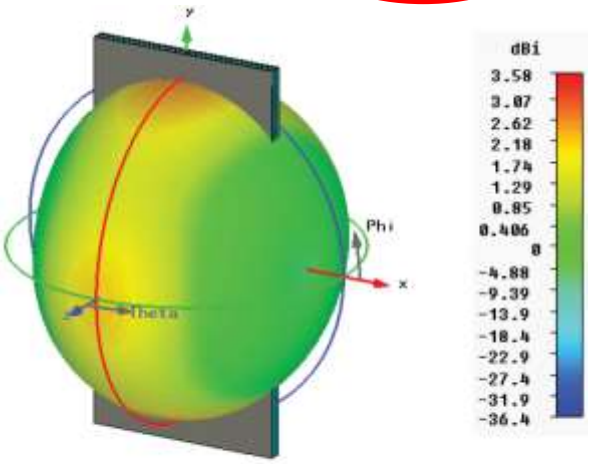
9.4.1 Radiation from a split plane (simu)







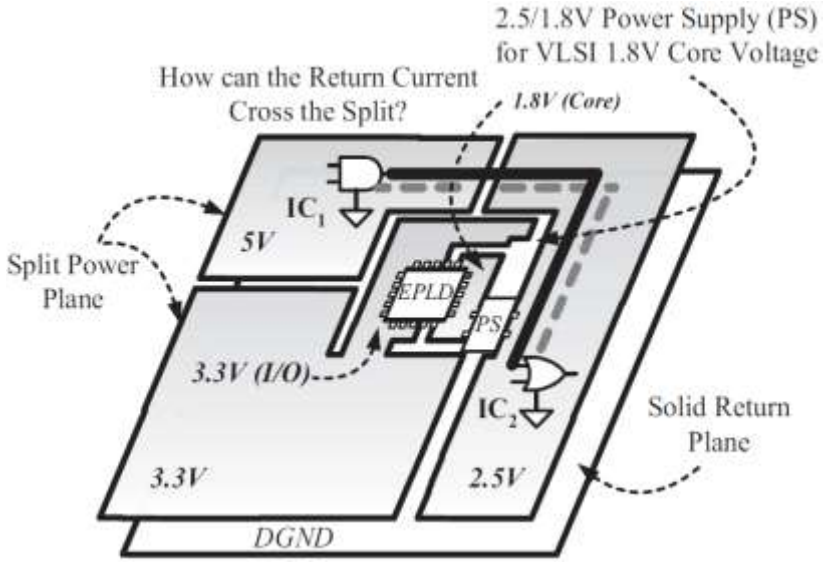
(a) Solid Plane Stripline Case, Directivity: [illegible]
Note: Total Radiation efficiency: 10^{-11}

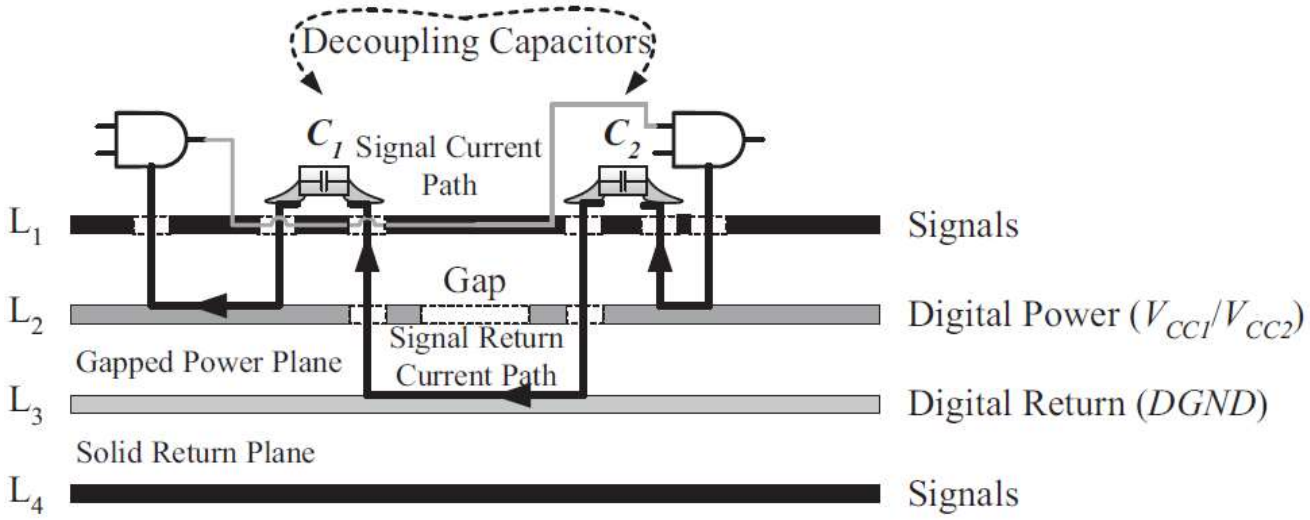


(B) Split Plane Stripline Case, Directivity: [illegible]
Note: Total Radiation efficiency: 2×10^{-2}

- Split plane is exactly a slot antenna that radiates very efficiently.

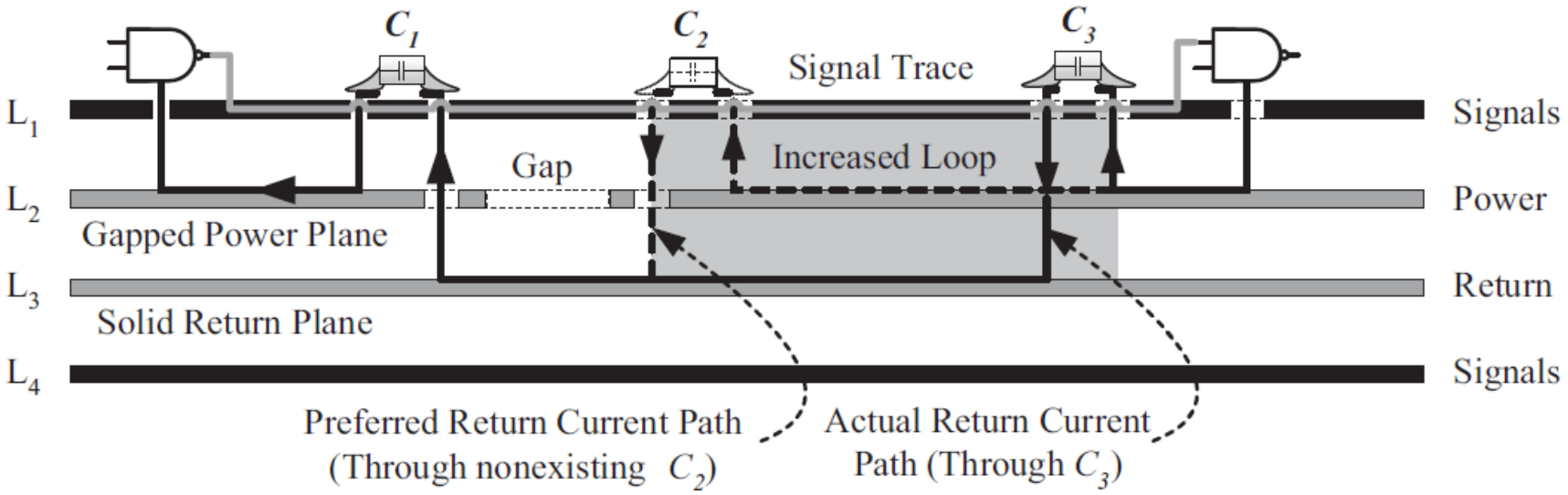
9.4.2 Traces cross different supply voltages





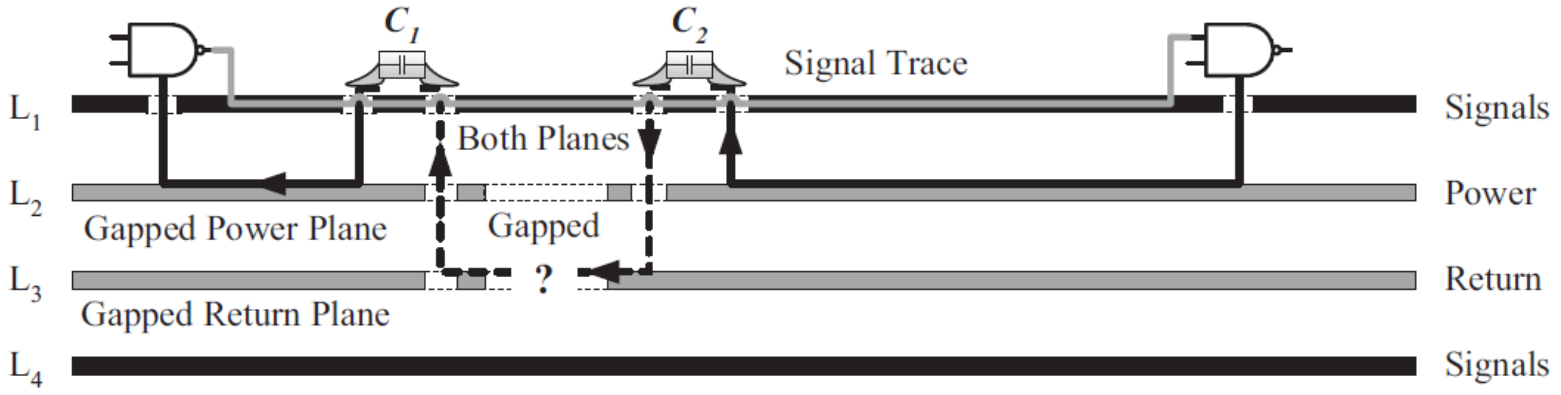
- Best approach: avoid routing traces across slots.
- Decoupling capacitors provide a natural return path.
- Attention, as we will see, in some cases, it doesn't work.

9.4.2 Traces cross different supply voltages

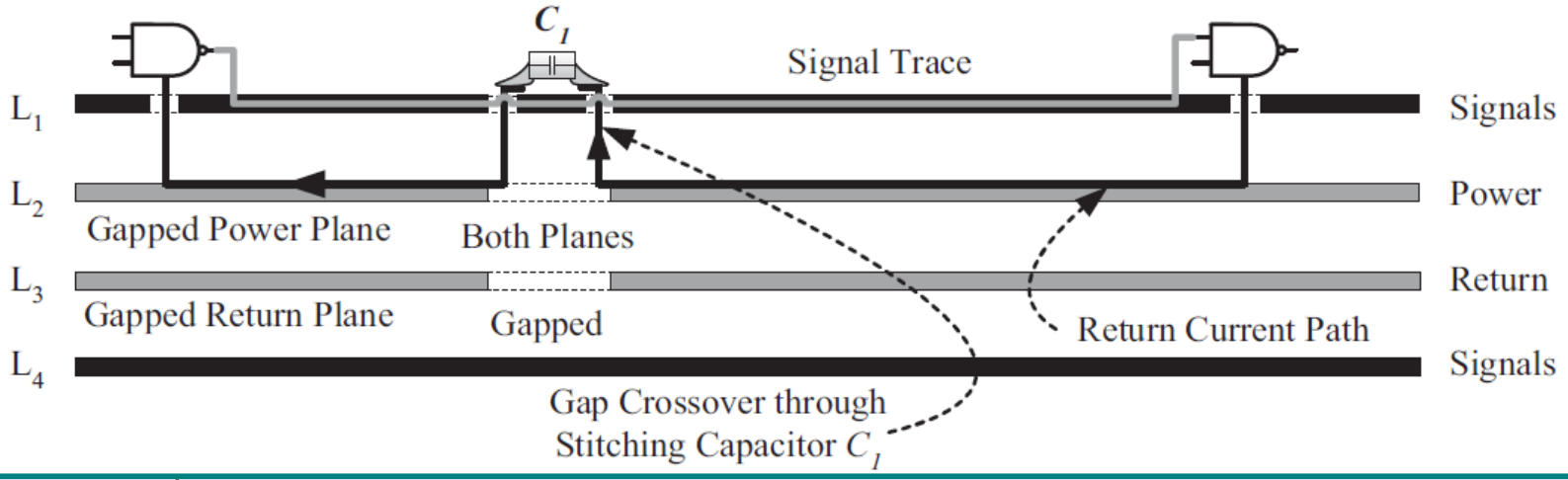


- C_3 is quite away from the gap.
- This creates a loop of increased size.
- Adding C_2 near the gap reduces the loop.

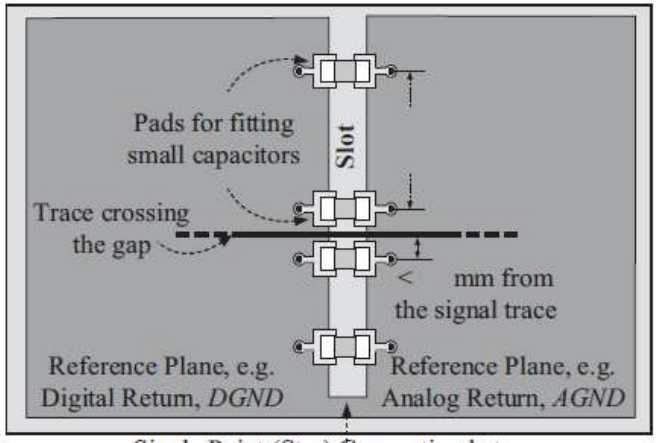
9.4.2 Traces cross different supply voltages



- If the return plane is also gapped, decoupling capacitors are useless.
- The solution is to uses “stitching” capacitors as follows.

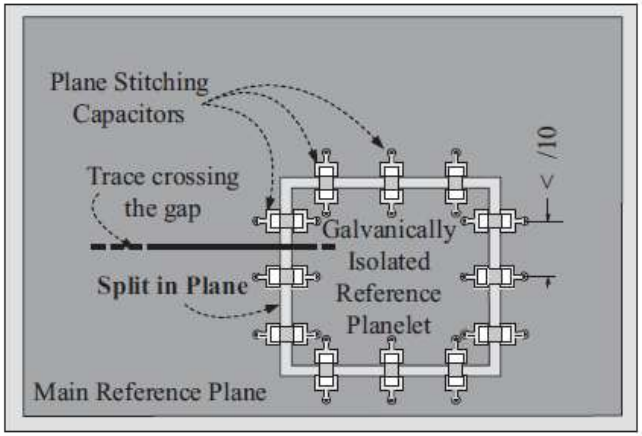


9.4.2 Capacitor placement



Single Point (Star) Connection between *AGND* and *DGND* Reference Planelets

(a) Stitching Capacitors across a Slot in a Reference Plane



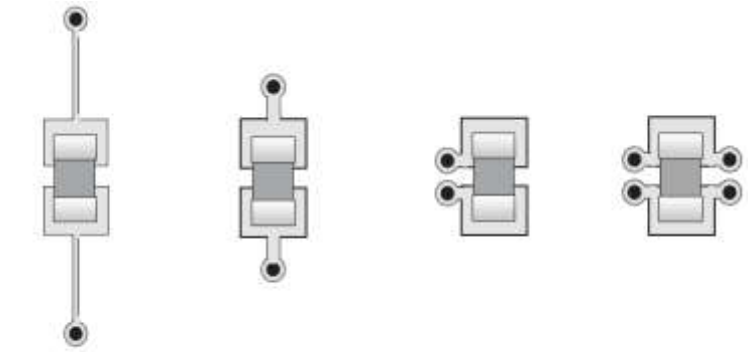
(b) Stitching Capacitors across a Slot in a Split Plane

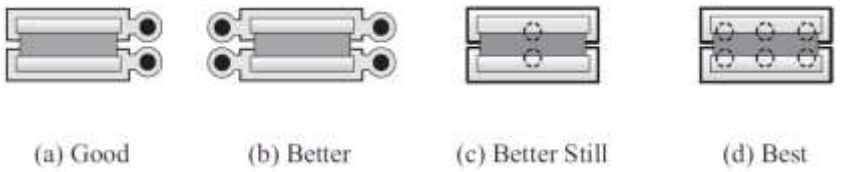
- Stitching capacitors across a slot in a reference plane.
- Capacitors regularly spaced.
- Increase capacitors density where the trace crosses the gap.

- In case of a planelet, capacitor are regularly spaced.

[Keith Amstrong, Cherry Clough]

9.4.2 Capacitor connection





Regular Aspect **Reverse Aspect**

0805	1206	0508	0612
1,050	1,250	600	610

- Parasitic inductance (ESL) increases with package size.
- Reverse aspect halves the parasitic inductance.

Inductance in pH

[Keith Amstrong, Cherry Clough]

9.4.2 Effect on radiated emission

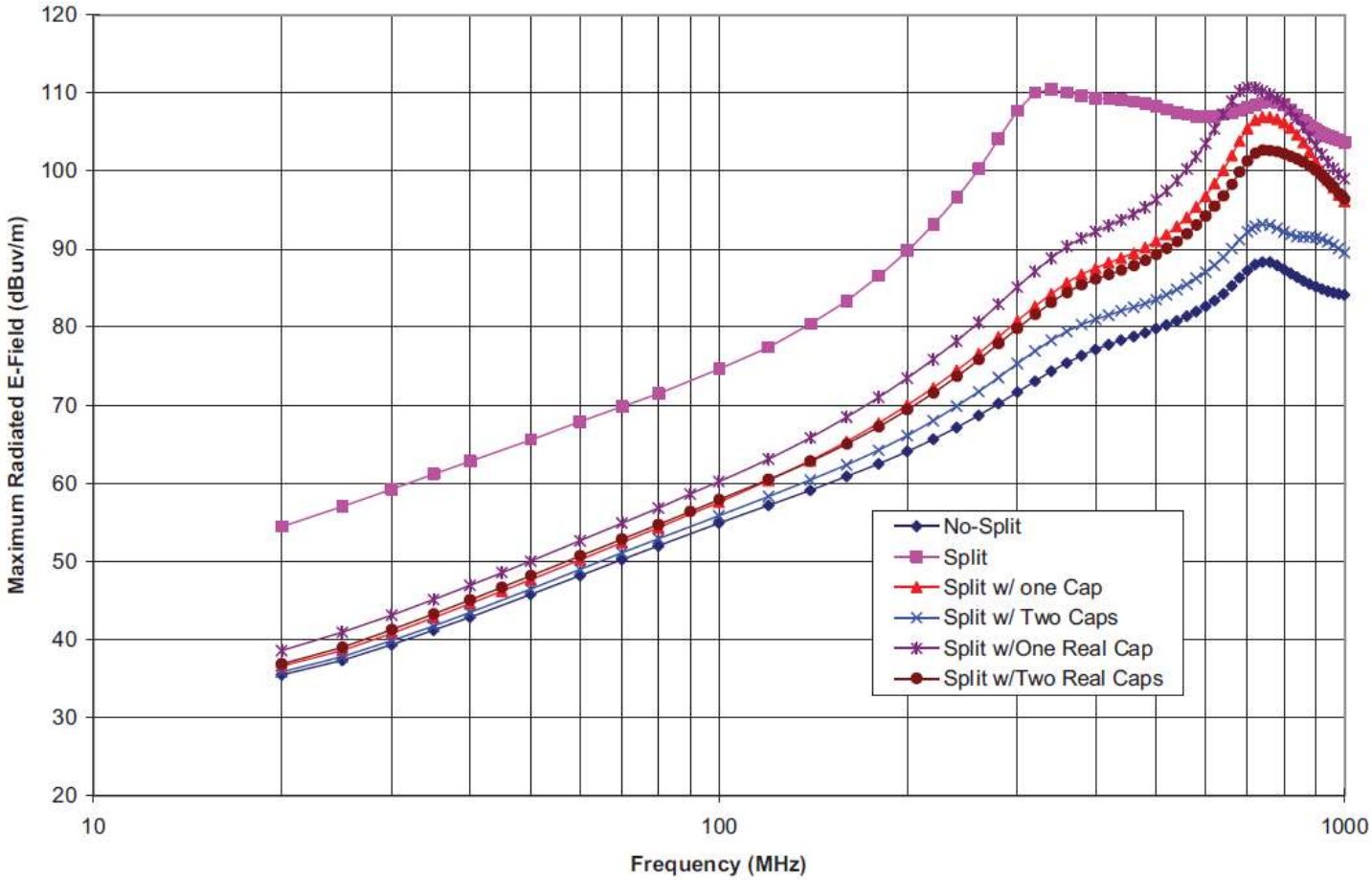
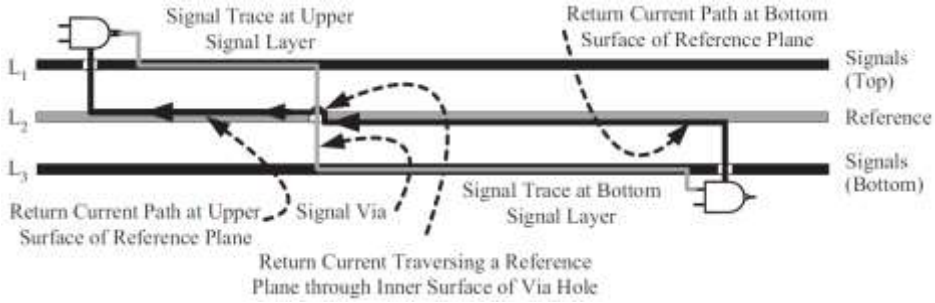
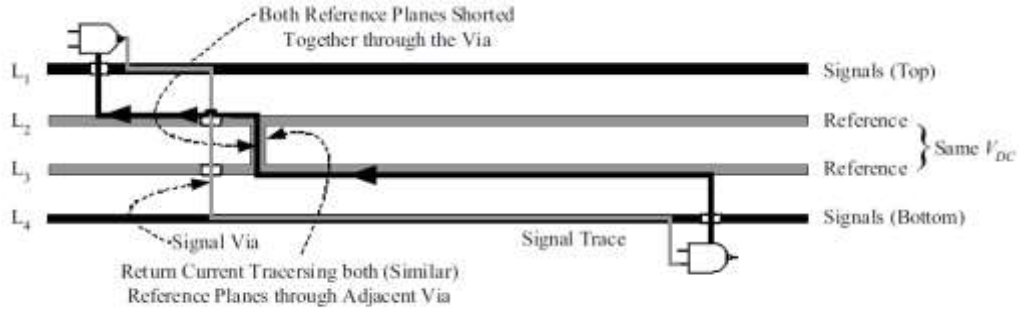


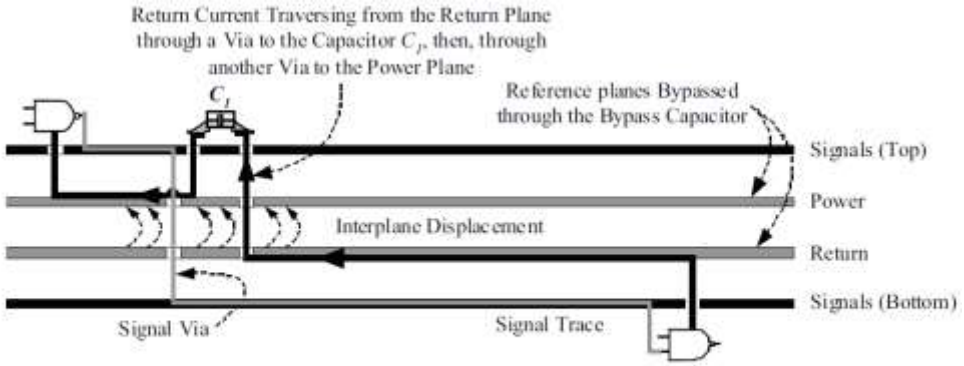
Figure 9.75. Maximum radiated E-field from a microstrip with and without a split in the reference plane and with ideally and real-world mounted stitching capacitors. (Courtesy of Bruce R. Archambeault, IBM Corporation.)

9.4.2 Traces jumping layers





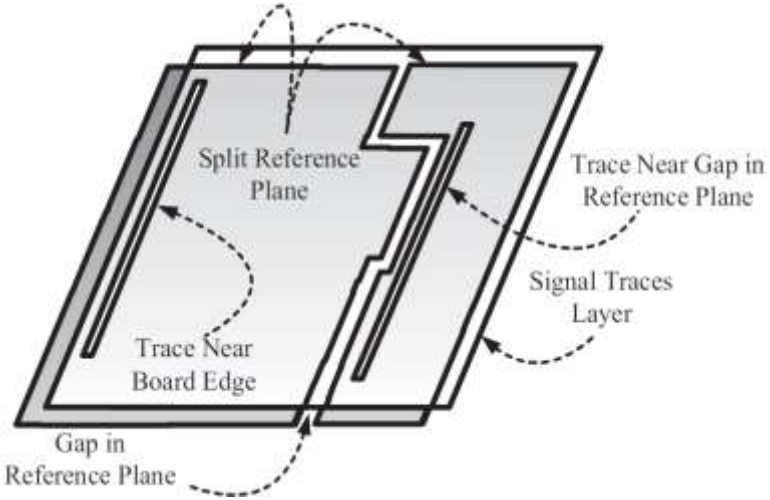
(a) Return Current Traverses through Via between Reference Planes of the Same DC Potential

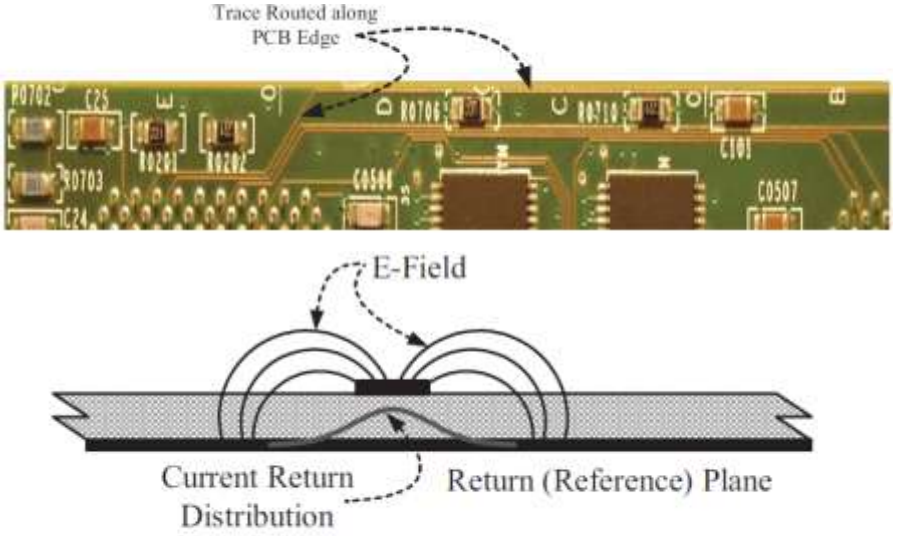


(b) Return Current Traverses through a Bypass Capacitor between Reference Planes of Different DC Potential (e.g., V_{CC} and GND)

- ✓ Same plane => no problem
- ✓ Different planes, same VDC => use vias at the transition location
- ✓ Different planes => use stitching capacitors **near transition**

9.4.2.6 Reference plane edge effect

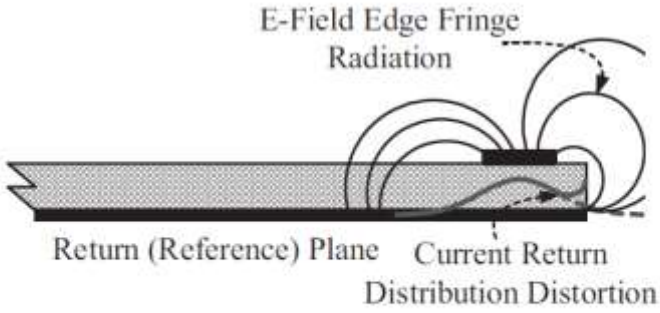




(a) Acceptable: Trace Far from Edge of Reference Plane

- There are TWO types of edges:
  1. board edge,
  2. reference plane gap edge.

- Return current is altered:
  1. EMI generation,
  2. immunity reduced,
  3. impedance increased (L increased).



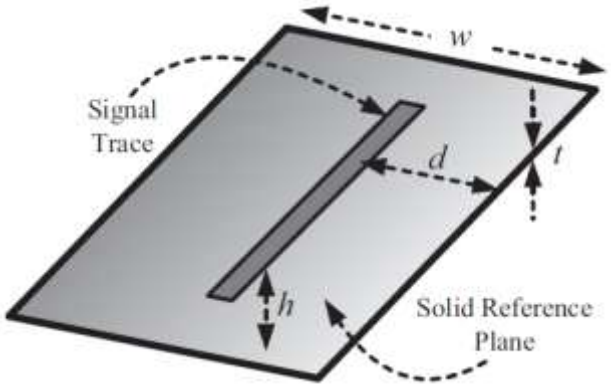
(b) Objectionable: Trace Adjacent to Edge of Reference Plane

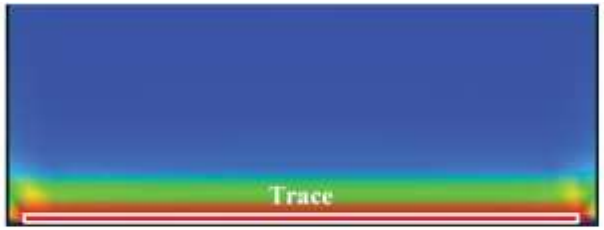
9.4.2.6 Reference plane edge effect

- Rule:

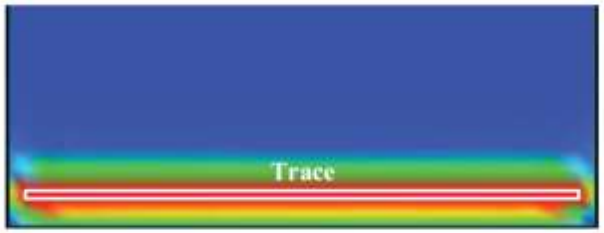
$$d \geq 10.h,$$

d is the distance to the edge,
h is the height of the trace above plane.





(a) Trace Separation of 0 mil from Edge of Plane

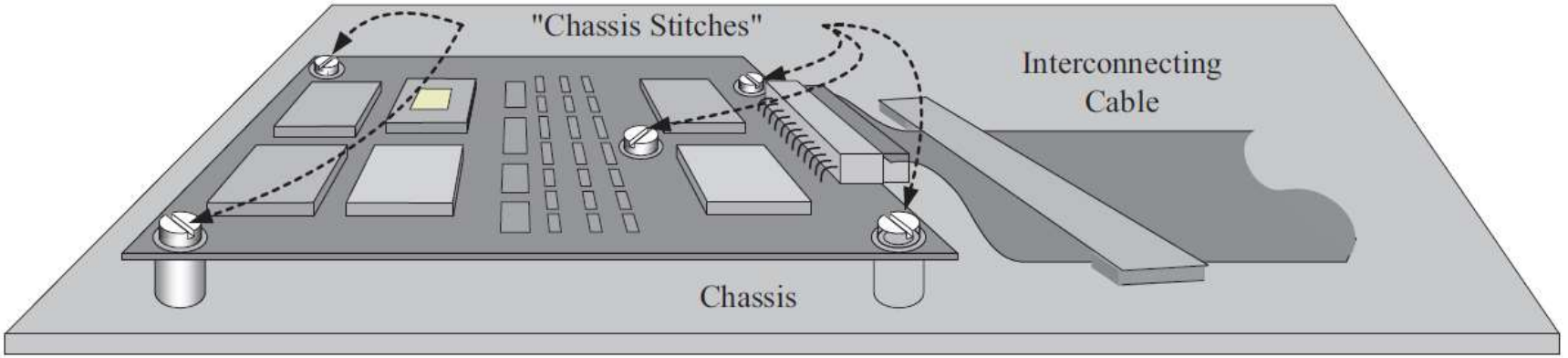


(b) Trace Separation of 30 mil from Edge of Plane

Figure 9.109. Simulation results visualizing the return current distribution in a solid reference plane under a signal trace at various separations from edge of the PCB at F = 100 MHz. (Simulation run on Agilent Technologies "Momentum" 3D Planar EM Simulator; courtesy of Alexander Perez, Agilent Technologies.)

9.9 Chassis connections (“stitching”)

- Connection to the chassis can improve RF performance by lowering the impedance of the ground plane (return plane).
- The “massive” chassis is a low impedance.
- **Typical connections** :
  - ✓ each **corner** of the PCB,
  - ✓ **I/O zones** (attention, very close to the output),
  - ✓ **boundary** between digital and analog/video/rf,
  - ✓ **near noisy sources** (clocks oscillator, noisy VLSI, DSP, CPLD),
  - ✓ source/emitter of switching devices.



[Keith Amstrong, Cherry Clough]

9.9.1 Purpose of stitching PCB return planes

- Reduction of EMI by impedance lowering.
- Improve immunity, especially to **ESD**.

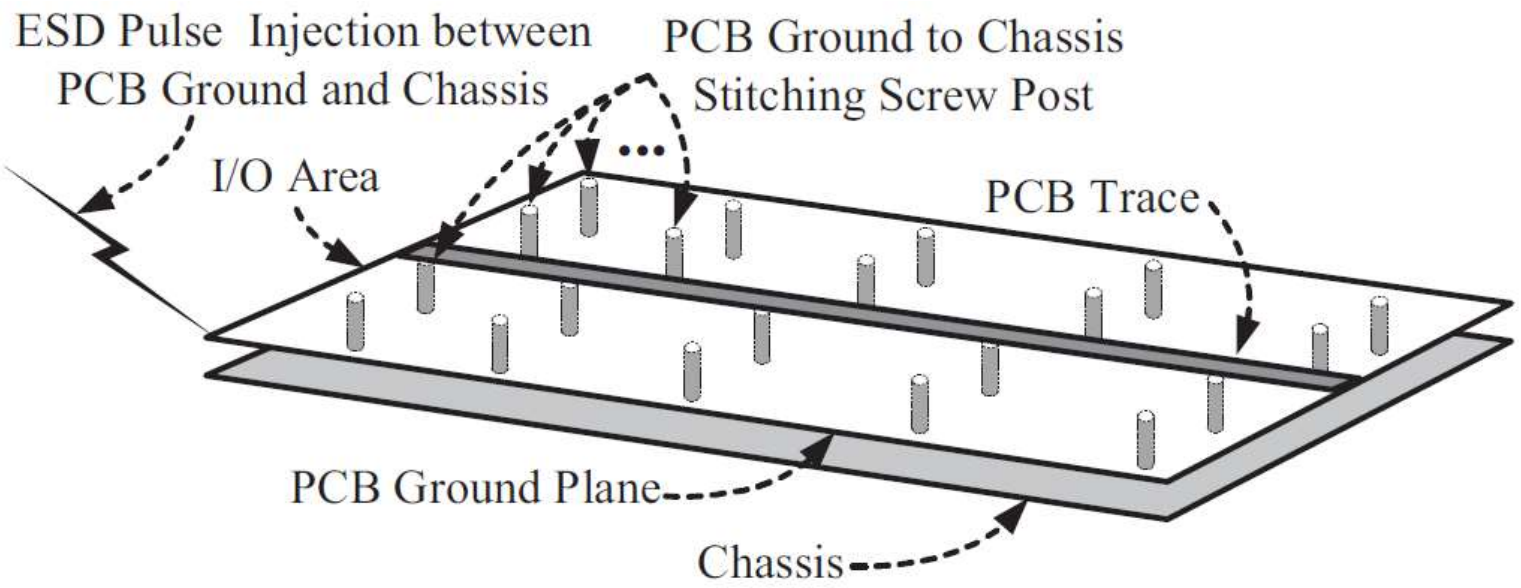


Figure 9.246. Distributed PCB ground plane to chassis stitching posts is important for control of ESD pulse propagation.

Figure 9.247. With only one stitching post at the left-hand I/O area, high levels of ESD pulse reflections are observed. (Courtesy of Dr. Bruce Archambeault.)

Figure 9.249. With four stitching posts placed at both ends of the PCB, lower levels of ESD pulse reflections are observed but propagation across the PCB still occurs. (Courtesy of Dr. Bruce Archambeault.)

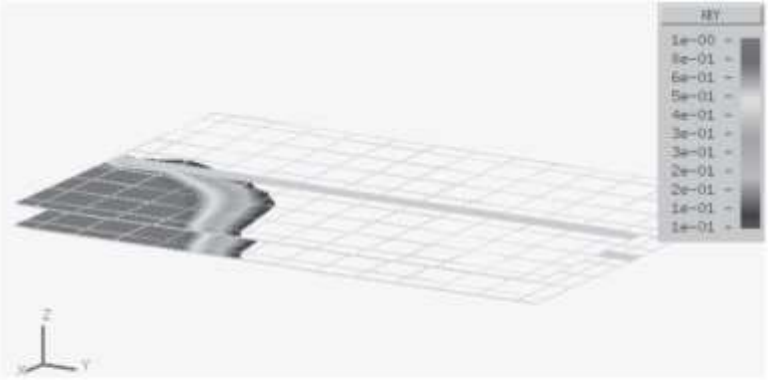


Figure 9.250. Evenly distributing the eight stitching posts throughout the PCB suppresses the ESD pulse, containing it near the injection area. (Courtesy of Dr. Bruce Archambeault.)

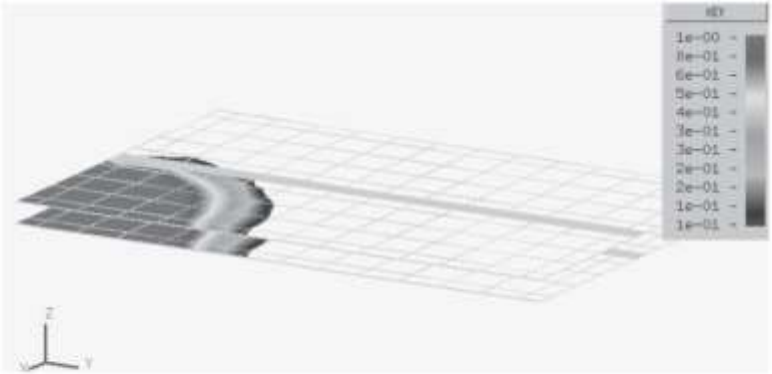
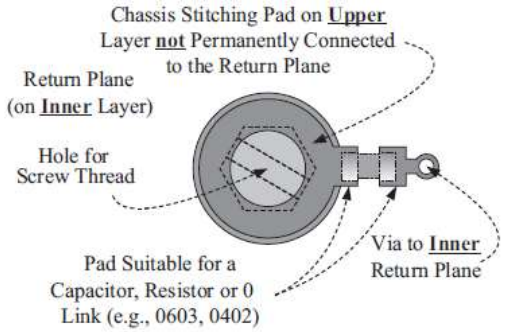
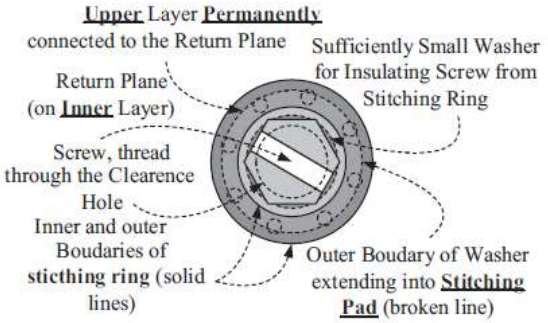


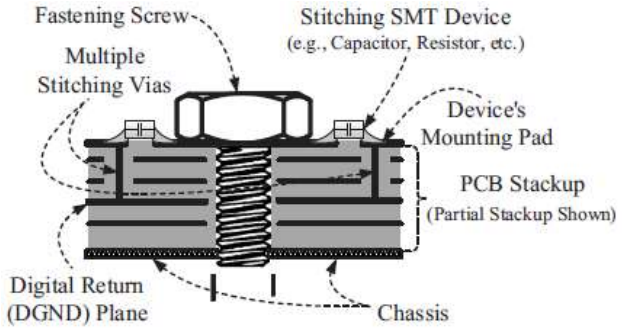
Figure 9.251. Increasing the number of evenly distributed stitching posts to 20 provides marginal improvement. (Courtesy of Dr. Bruce Archambeault.)



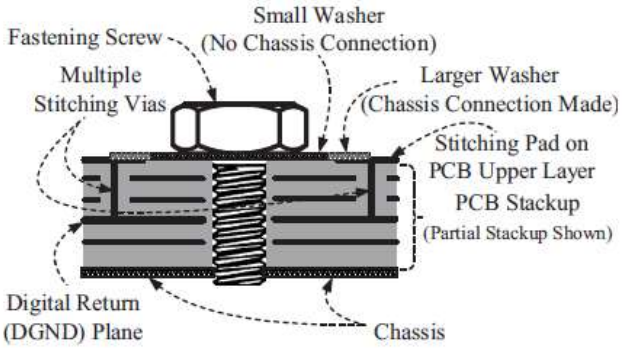
(a) Interconnecting the Return Plane and Chassis Stitching Pad through a SMT Device. (Courtesy of *Keith Armstrong, Cherry Clough)*



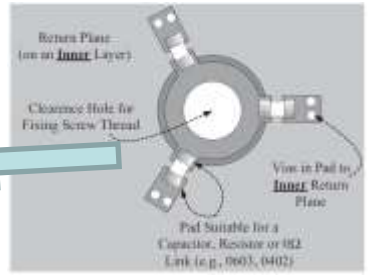
(b) Interconnecting the Return Plane and Chassis Stitching Pad through Conductive Fixing Washers



(c) Detailed Side View of the Return Plane and Chassis Stitching Pad through a SMT Device



(d) Interconnecting the Return Plane and Chassis Stitching Pad through Conductive Fixing Washers



Electro-chemical corrosion !

- Keep some **flexibility** during design (connection, capa., resistive, open).
- Location, manner and number of chassis connection is not always straightforward .

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