Computation Structures — Tutorial 11

December 4, 2018

A Performance-Oriented β Machine

1. Give the values of the various signals generated by the control logic when executing the following instructions: `LD`, `ADD`, `BEQ`.

2. Is it possible to add the following instructions to the instruction set of the μ-code-less β machine? If yes, give the values of the various signals generated by the control logic when executing this instruction. Else, just explain why it cannot be implemented.

   (a) `PUSH(Rc, 4, Ra)`:
   ```
   PC <- PC + 4
   Mem[Reg[Ra]] <- Reg[Rc]
   Reg[Ra] <- Reg[Ra] + 4
   ```

   (b) `LDA(Ra, Rb, Rc)`:
   ```
   PC <- PC + 4
   EA <- Reg[Ra] + Reg[Rb]
   Reg[Rc] <- Mem[EA]
   ```

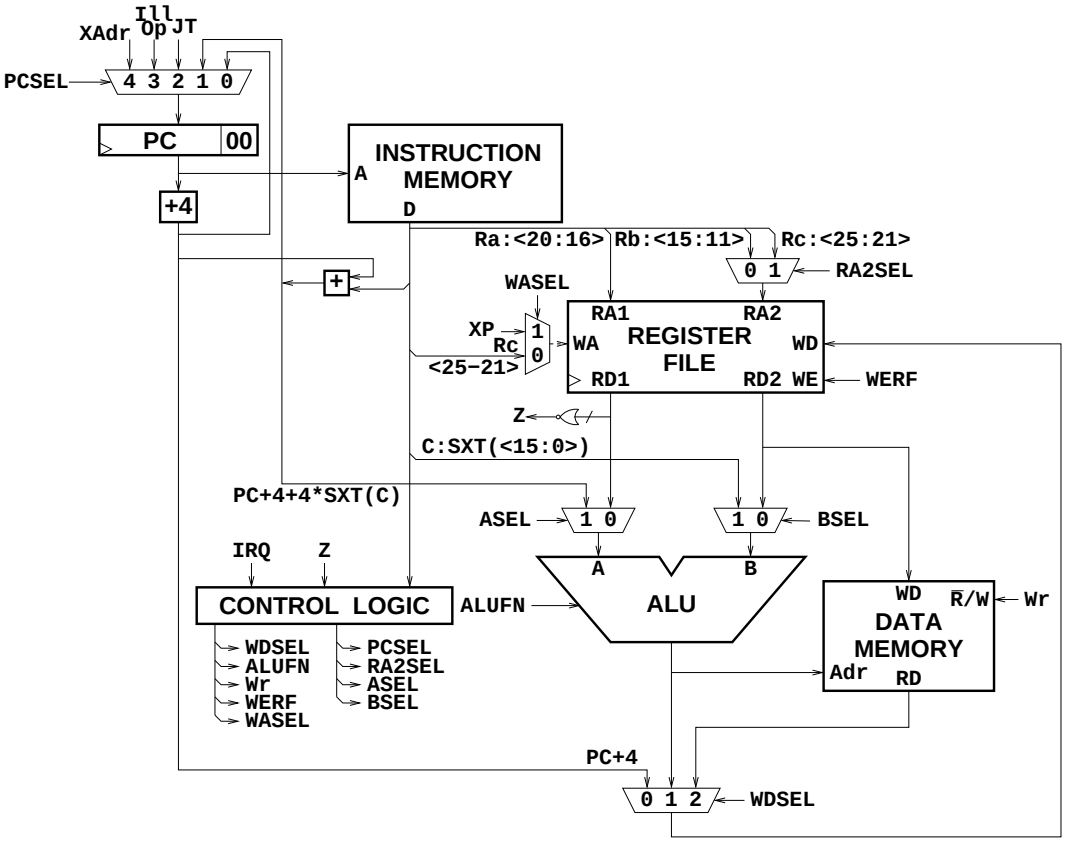
   (c) `STA(Ra, Rb, Rc)`:
   ```
   PC <- PC + 4
   EA <- Reg[Ra] + Reg[Rb]
   Mem[EA] <- Reg[Rc]
   ```

   (d) `MVEQ(Ra, Rb, Rc)`:
   ```
   PC <- PC + 4
   if Reg[Ra] = 0 then Reg[Rc] <- Reg[Rb]
   ```

   (e) `MVCEQ(Ra, literal, Rc)`:
   ```
   PC <- PC + 4
   if Reg[Ra] = 0 then Reg[Rc] <- SEXT(literal)
   ```

   (f) `SWAP(Ra, literal, Rc)`:
   ```
   PC <- PC + 4
   EA <- Reg[Ra] + SEXT(literal)
   TMP <- Mem[EA]
   Mem[EA] <- Reg[Rc]
   Reg[Rc] <- TMP
   ```

   (g) `TCLR(Ra, literal , Rc)`:
   ```
   PC <- PC + 4
   EA <- Reg[Ra] + SEXT(literal)
   Reg[Rc] <- Mem[EA]
   Mem[EA] <- 0
   ```


Ill Op
XAdr
JT
PCSEL
4 3 2 1 0
PC
00
+4
INSTRUCTION MEMORY
A
D
Ra:<20:16>
Rb:<15:11>
Rc:<25:21>
0 1
RA2SEL
+
WASEL
XP
Rc
<25-21>
1
0
RA1
RA2
WA
REGISTER FILE
WD
RD1
RD2
WE
WERF
Z
C:SXT(<15:0>)
PC+4+4*SXT(C)
ASEL
1 0
1 0
BSEL
IRQ
Z
A
B
CONTROL LOGIC
ALUFN
ALU
WD
R/W
Wr
DATA MEMORY
Adr
RD
WDSEL
ALUFN
Wr
WERF
WASEL
PCSEL
RA2SEL
ASEL
BSEL
PC+4
0 1 2
WDSEL