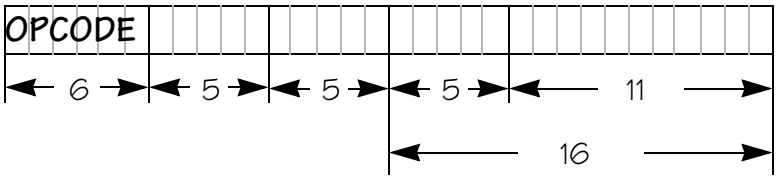
BETA Architecture for 6.004: Instruction Formats - 10/97 SAW



Operate class: $R_c \leftarrow$ $<R_a>$ op $<R_b>$

Operate class: $R_c \leftarrow$ $<R_a>$ op C

Opcodes, both formats:

ADD	SUB	MUL*	DIV*	*optional
CMPEQ	CMPLE	CMPLT		
AND	OR	XOR		
SHL	SHR	SRA		

LD: $R_c \leftarrow$ Mem[$<R_a>$ + C]

ST: Mem[$<R_a>$+C] $\leftarrow$ $<$Rc$>$

JMP: $R_c \leftarrow$ $<$PC$>$+4; PC $\leftarrow$ $<R_a>$

BEQ: $R_c \leftarrow$ $<$PC$>$+4; if $<$Ra$>$=0 then PC $\leftarrow$ $<$PC$>$+4+(C<<2)

BNE: $R_c \leftarrow$ $<$PC$>$+4; if $<$Ra$>\neq$0 then PC $\leftarrow$ $<$PC$>$+4+(C<<2)

LDR: $R_c \leftarrow$ $<<$PC$>$+4+(C<<2)$>$

Opcode Map: (* optional)

	000	001	010	011	100	101	110	111
000								
001								
010								
011	LD	ST		JMP		BEQ	BNE	LDR
100	ADD	SUB	MUL*	DIV*	CMPEQ	CMPLT	CMPLE	
101	AND	OR	XOR		SHL	SHR	SRA	
110	ADDC	SUBC	MULC*	DIVC*	CMPEQC	CMPLTC	CMPLEC	
111	ANDC	ORC	XORC		SHLC	SHRC	SRAC	